Paralleling SiC Cascode JFETs

Best Practices

AND90327/D

SCOPE

This document provides application information for the **onsemi** SiC cascode JFETs to assist the user in paralleling for higher current operation. Included is a description of key cascode parameters, parallel oscillation, and design guidelines.

INTRODUCTION

Operation at high current often requires direct paralleling of power semiconductor parts. Paralleling discrete parts is often desirable for cost and/or physical layout reasons. The alternative is power modules, but even these use paralleled chips. Included here are common best practices applicable to paralleling voltage-gated power semiconductors of any technology, be it SiC Cascode JFET, SiC MOSFET, Si MOSFET, IGBT, etc. Paralleling high gain parts such as a cascode is particularly challenging. These best practices help to achieve successful paralleling of SiC JFET cascodes.

CASCODE BACKGROUND INFORMATION

Showing in Figure 1, the cascode is made by series-connecting a normally-on SiC JFET with a low-voltage Si MOSFET. The JFET gate connects directly to the MOSFET source, with the JFET gate resistance part of the JFET chip. The MOSFET drain-source voltage is the inverse of the JFET gate-source voltage so that the cascode has a familiar normally-off characteristic. As explained in the Cascode Primer, a key difference between the cascode and other power transistors is the lack of gate-drain capacitance, once V_{DS} exceeds the JFET threshold voltage. This is because the JFET has no drain-source capacitance, resulting in very fast switching in the cascode configuration. This characteristic in combination parasitic inductances is central to the operation of parallel cascodes.

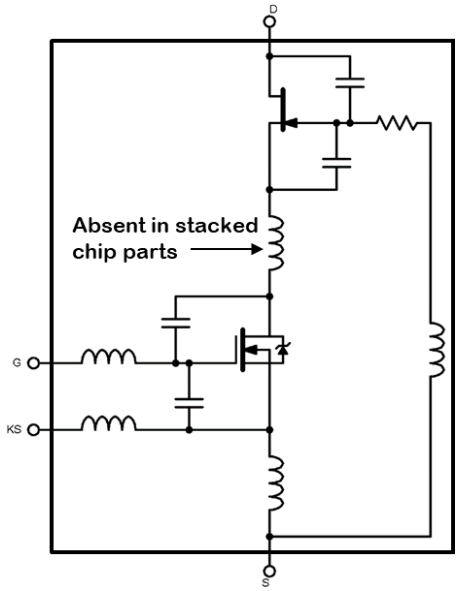

Figure 1. Cascode Structure with Stray Impedances

CHALLENGES TO PARALLELING

Static Current Mismatch

Static current mismatch is a mismatch in current between parallel parts after switching transients have settled. This is especially a concern for parts with inherent thermal instability, or in other words, parts with a negative temperature coefficient of on-resistance as in older Si diodes and punch-through IGBTs. Parts with a negative TC can be successfully paralleled if the part-to-part variation (distribution) of on-resistance is sufficiently narrow (binned parts) and margin is added to account for inevitable current mismatch.

There is a widespread myth that a positive temperature coefficient in on-resistance forces uniform current sharing and consequently facilitates paralleling. In reality, a positive TC *only ensures thermal stability*. The belief in the power of a positive TC over current sharing is reinforced by the narrow parameter distributions of modern power semiconductors, including SiC JFETs, SiC MOSFETs, field stop IGBTs, etc. It is parameter distribution and common heat sinking that determine static current sharing.

Dynamic Current Mismatch

Dynamic current mismatch is caused by part-to-part threshold voltage variation that is inherent in MOS-gated and JFET devices, by asymmetry in current loops, and by variation in propagation delay between gate drivers if applicable. A part with lower threshold voltage switches on sooner and off later and consequently has more hard-switching loss. This is more of a concern at very high switching frequencies.

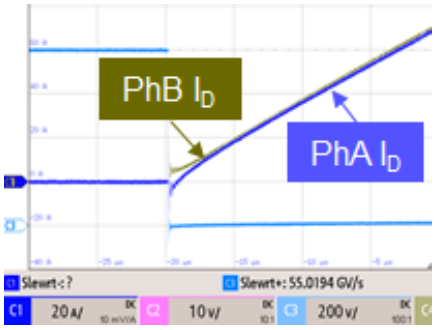

Figure 2. Dynamic Current Mismatch Due to Threshold Voltage Mismatch

Figure 2 shows the dynamic mismatch at turn-on of two parallel cascodes. The current mismatch quickly shrinks, which is typical because steady state current sharing is dominated by $R_{DS(on)}$. Using maximum $R_{DS(on)}$ and $R_{\theta JC}$ datasheet values in calculations provides safety margin to accommodate static and dynamic current mismatch when paralleling.

Parallel Oscillation

Parallel oscillation can be a problem with high gain, fast switching parts. This is especially a concern with the SiC JFET cascode (hereafter known as cascode for short) due to two active devices inside: a low-voltage Si MOSFET and a SiC JFET. Sustained parallel oscillation, as in Figure 3, risks device failure due to exceedingly high switching loss. It can be difficult to observe the oscillation with an oscilloscope. Waveforms can look fine, and within only a couple switching cycles, oscillation can begin. There are various possible causes for this, such as variations in load current, voltages, and temperature. It is mainly caused by the fast switching of the cascode, especially at high current when di/dt and dv/dt become even faster.

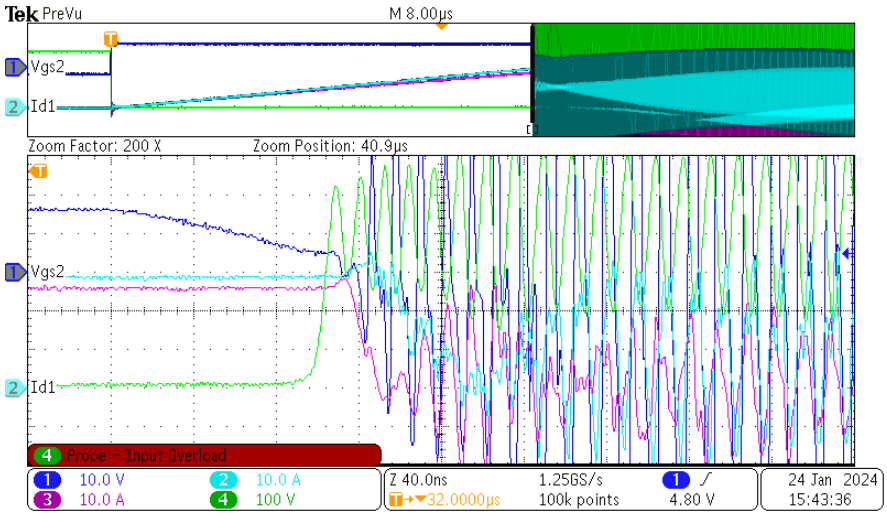

Figure 3. Two Parallel Cascodes Going into Sustained Parallel Oscillation During Double-pulse Testing

Despite the complexity, it is useful to analyze the operation of two parallel cascodes including relevant capacitances and inductances, as shown in Figure 4 for cascodes with a Kelvin-source pin. The TO-247-3L and D2Pak-3L packages have no Kelvin-source pin, and this situation is discussed later.

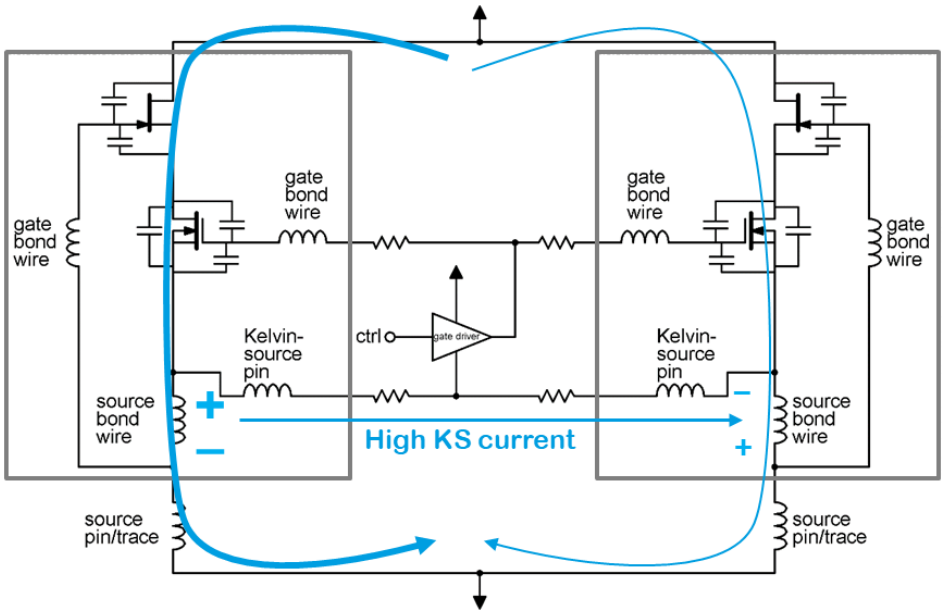

Figure 4. Two Parallel Cascodes Turning On with Dynamic Current Mismatch

As already mentioned, dynamic current mismatch is practically unavoidable due to variations in threshold voltages, and possibly compounded by asymmetry in the circuit layout. In Figure 4, we can imagine two cascodes switching on, with the one on the left switching on slightly sooner than the one on the right. Higher current in the left cascode causes higher voltage to develop across the left side source inductances. In extreme cases, current in the right cascode can flow momentarily in the reverse direction. In any case, the source voltage mismatch induces current to flow through the Kelvin-source connections, as indicated in Figures 4 and 5.

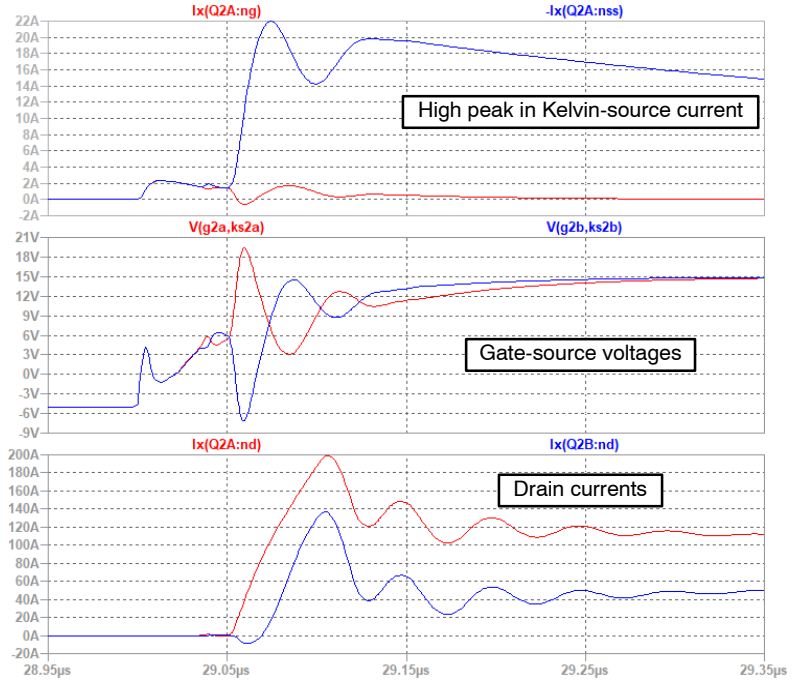

Figure 5. Top: Kelvin-source Current Greatly Surpasses Gate Current Middle and Bottom: V_{GS} and I_D of Each Cascode

Figure 5 shows the simulation results of two parallel UF3SC120009K4S hard-switching on with an inductive load. Each part has a 680 pF plus 4.7 Ω drain-source snubber. One cascode has 10% lower than typical and the other 10% higher than typical threshold voltage for both the JFET and MOSFET, thus inducing dynamic current mismatch. This is a plausible situation, even if unlikely. There is no added Kelvin-source impedance. The top graph shows high peak Kelvin-source current greatly surpassing the cascode gate current. Ideally, the gate and Kelvin-source currents are equal in magnitude (differential). The cascode gate-source voltages in the middle graph show out of phase ringing, a tell-tale indicator of imbalanced gate-source voltages, which under certain circumstances can escalate into a sustained, destructive parallel oscillation. The bottom graph of Figure 5 shows the mismatch in drain currents that ultimately causes the large Kelvin-source current. The dynamic current mismatch settles to near zero steady state.

Source and/or drain inductance mismatch also causes dynamic mismatch. Combining this with random threshold voltage variations can make parallel oscillation occur randomly, especially with a cascode because both JFET and MOSFET threshold voltage variation cause dynamic current mismatch.

A seemingly simple solution is to move all the gate loop resistance to each Kelvin-source connection, or as much as possible if different turn-on/off resistances are used, as shown in Figure 6(b). This can however result in sustained oscillation. Why? The peak Kelvin-source current is certainly reduced by the increased Kelvin-source resistance. However, consider that the charge to/from the gate-drain capacitance of the cascode's MOSFET is through the cascode's gate resistor. Less gate resistance allows higher peak gate current, higher peak dV_{DS}/dt of the MOFSET, and consequently higher peak dV_{GS}/dt of the JFET. Furthermore, the gate resistance provides damping for the MOSFET output capacitance – source inductance and other LC tank circuits. Moving all gate loop resistance to the Kelvin-source connection removes damping from the cascode's MOSFET gate, which combined with a large mismatch in gate versus Kelvin-source current can result in oscillation.

How can we maximize gate damping while minimizing the mismatch between gate and Kelvin-source currents? First, we leave the gate resistance for each cascode in the gate connection instead of in the Kelvin-source connection. We need to maximize damping of each gate, so no common gate resistor should be used, see Figure 6(a). Put all gate resistance in each cascode gate connection. Follow the User Guide recommendations of gate resistor values for initial testing. Second, we could add a common-mode choke (CMC) or differentially coupled inductors to the gate and Kelvin-source connections, as in Figure 7(a). This forces the gate and Kelvin-source current magnitudes to match more closely. Experiments demonstrated that sustained oscillations were eliminated with a CMC impedance of at least 100 Ω at 10 MHz, such as Pulse AWCU00453226223TT2, or Bourns SRF4530A-220Y, or similar. Exact values are not critical; especially because the CMC has no effect on delay times. Third, snubbers must be installed when paralleling. In addition to reducing switching slew rates, a snubber also damps ringing with the snubber resistor. Hence adding snubbers greatly reduces the likelihood of oscillation. Finally, minimize the gate resistance by relying on the snubbers to set the switching speed as much as possible. This is counterintuitive but is explained in the Cascode Primer. The User Guide gate resistor recommendations are minimal values for clean switching. Parallel parts can share a common snubber, or there can be a separate snubber for each cascode. The important points are layout symmetry and minimum inductance in the snubber connections.

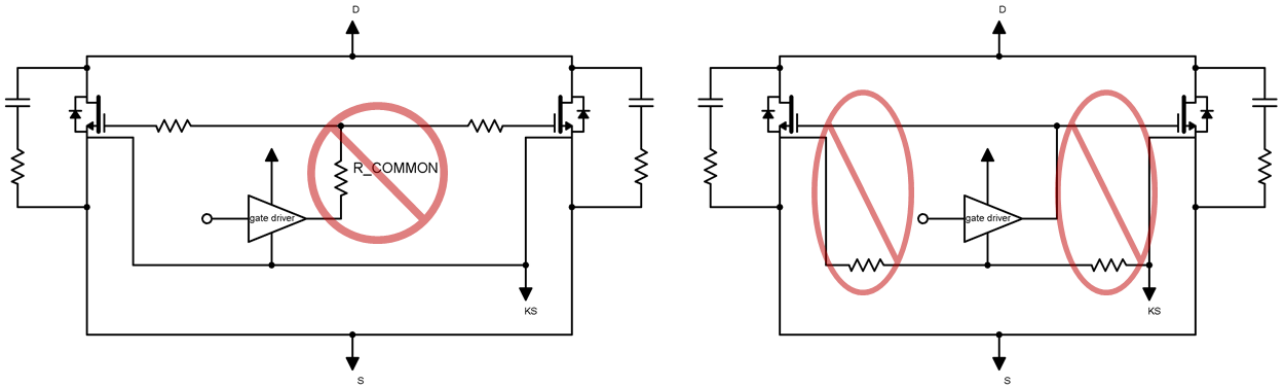

Figure 6. Things to Avoid when Paralleling

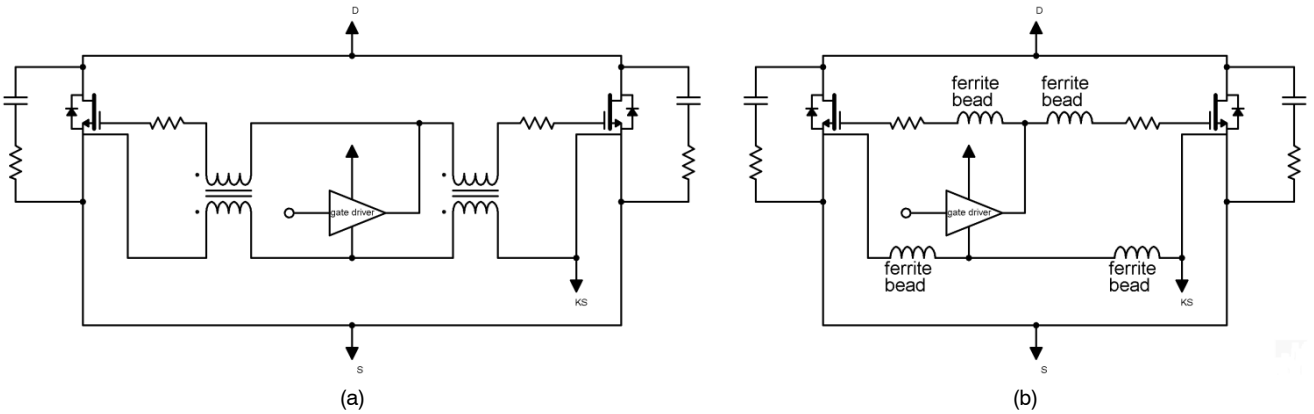

Figure 7. Recommended Paralleling Methods with Kelvin-source

Routing of traces can be challenging with common-mode chokes. A ferrite bead on the other hand can be very small and easier to fit in a tight board layout, as in Figure 7(b). A ferrite bead in each Kelvin-source and gate connection works to avoid oscillation, as with a CMC. Unlike the CMC, however, the ferrite beads cause a noticeable increase in delay times. Recommended impedance range is 70 to 400 Ω at 100 MHz, such as Bourns MU2029-301Y. As with the addition of CMCs, prevention of oscillations was demonstrated with a ferrite bead in both the Kelvin-source and gate connections in addition to the usual gate resistor in the gate connection.

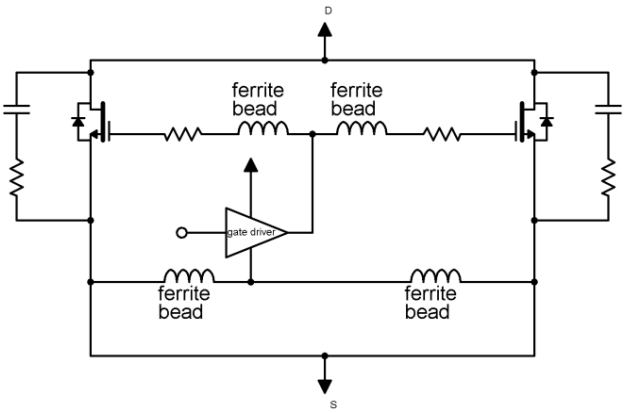

Figure 8. Recommended Paralleling Method without Kelvin-source

Parts Without Kelvin-Source

Paralleling parts without a Kelvin-source pin is possible. In general, however, it is better to parallel parts *with* a Kelvin-source pin because the elimination of load current in part of the gate drive loop greatly reduces gate ringing. Without a Kelvin-source pin, the recommendation is to install a ferrite bead in both the gate and the gate drive return connection to each cascode source, as shown in Figure 8. This drawing is conceptual only. Depending on the gate driver, when using a negative turn-off voltage, the gate drive return may connect to the gate drive power supply instead of directly to the gate driver.

Other Design Tips

As mentioned before, snubbers are usually required with cascodes, and they are especially needed when paralleling. The drain-source snubber reduces switching slew rates, making oscillation less likely to begin. See the User Guide for more information.

DC link capacitance and decoupling capacitance must be close to the cascodes to minimize inductance. Surface mount ceramic capacitors (DC link) next to the cascodes combined with bulk film and/or aluminum electrolytic capacitors (decoupling) is recommended.

Symmetrical power layout is important. High current, say greater than 100 A, with high di/dt slew rate can magnetically “push” current flowing in adjacent devices and conductors to one side, causing current imbalance and other noise related disturbances.

Sufficient bypass capacitance near the gate driver and its power supply is necessary; insufficient capacitance here can cause oscillations. Surface mount ceramic capacitors are recommended.

Gate traces *can* be long, and because we are generally not dealing with switching frequencies in the MHz range, they can be of different length without impact. Gate traces must however be shielded, preferably by a power plane on an adjacent circuit board layer. Never cross gate traces over power plane boundaries.

DEMONSTRATION AND TEST RESULTS

A demonstration board was designed following the guidelines mentioned above, and test results are shown for four devices:

- UJ4SC075006K4S
- UJ4C075023K4S
- UF3SC120009K4S
- UF3SC120016K4S

Demonstration Board Design

Figure 9 shows the demonstration and test setup, there are one half bridge topology power board with two devices in parallel and one gate driver board.

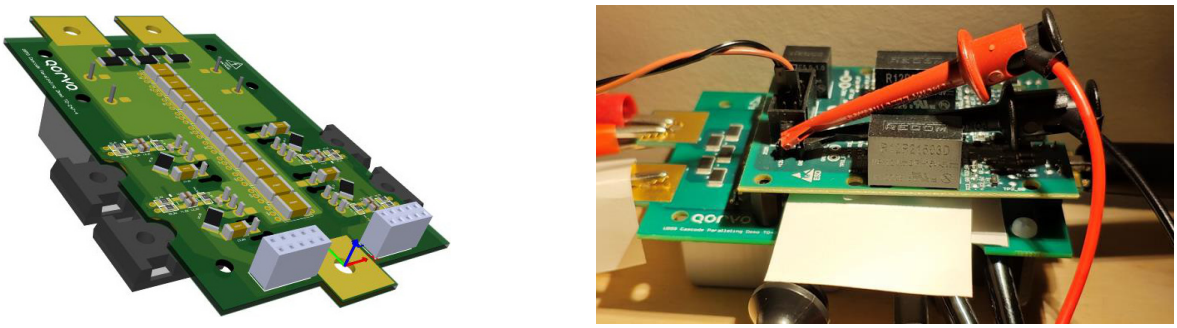

Figure 9. Demostration Board and Test Setup Picture

This demonstration adapts the recommendations of symmetric design of both power loop and gate drive circuits. Also, the DC link capacitor and the decoupling capacitors are symmetrical to minimize the commutation loop.

Figure 10 and 11 gives the schematics of demonstration design, the ferrite beads and common-mode choke are implemented (options) for exploration of effects under different conditions.

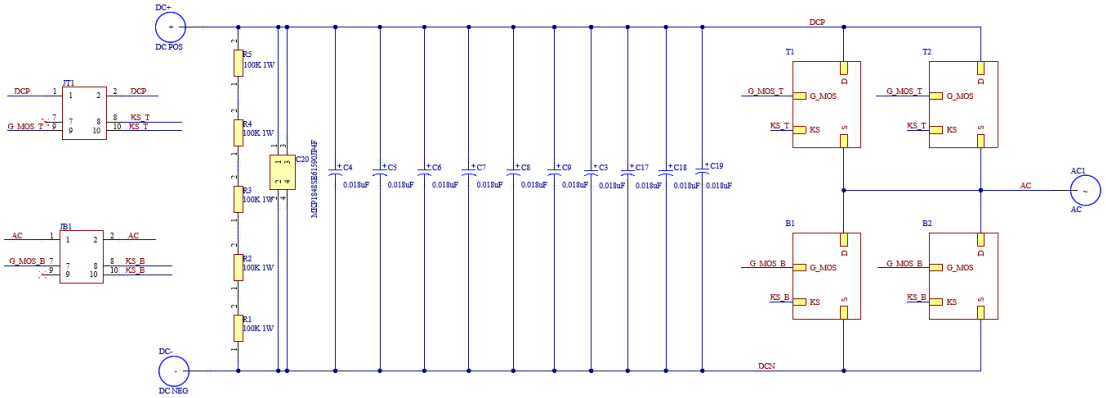

Figure 10. Demonstration Design Schematics

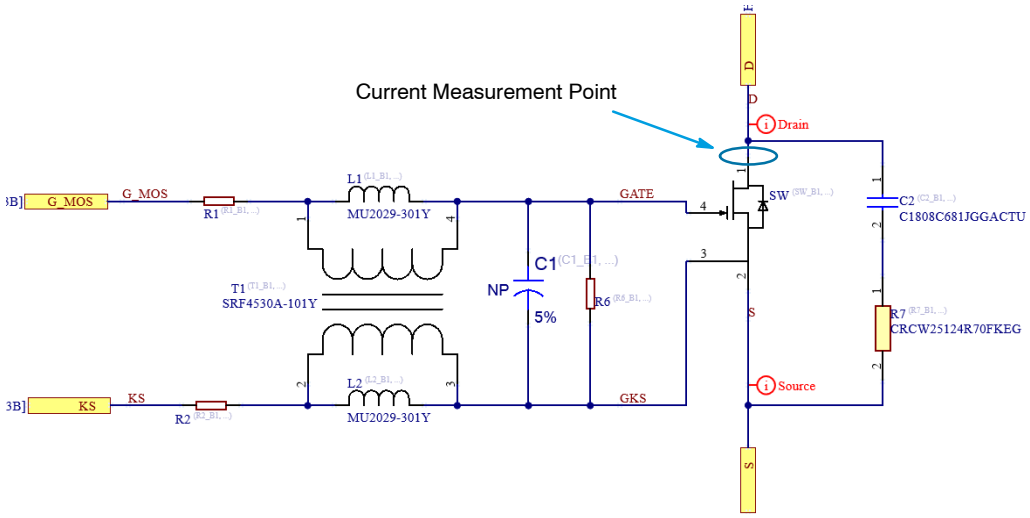

Figure 11. Demonstration Design Schematics

Figure 12 shows the PCB layout of the power board:

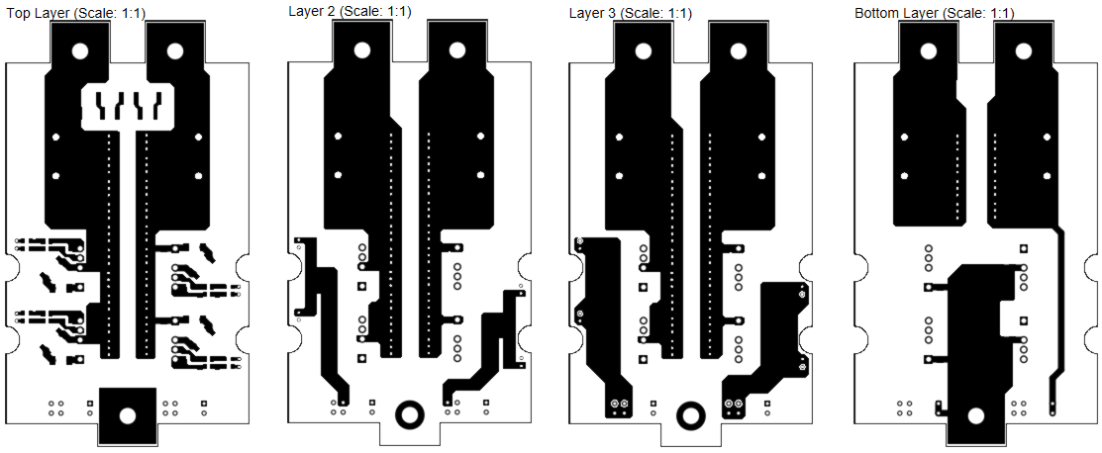

Figure 12. Demonstration Power Board PCB Layout

Figure 13 shows the demonstration design of device RC snubber and gate circuit layout, the key of this design example is to minimize the RC snubber distance to device and symmetric layout of gate circuit for devices in parallel.

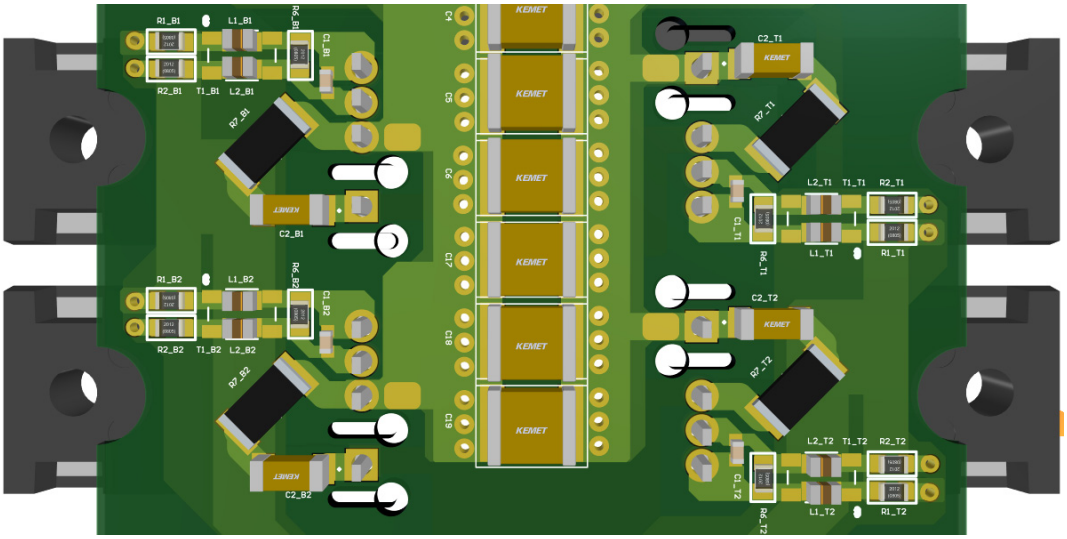

Figure 13. Demonstration Power Board PCB Layout

Test Results

Figure 14 to Figure 17 show the test results SiC FET paralleling of this demonstration design, with ferrite beads on both gate and Kelvin-source.

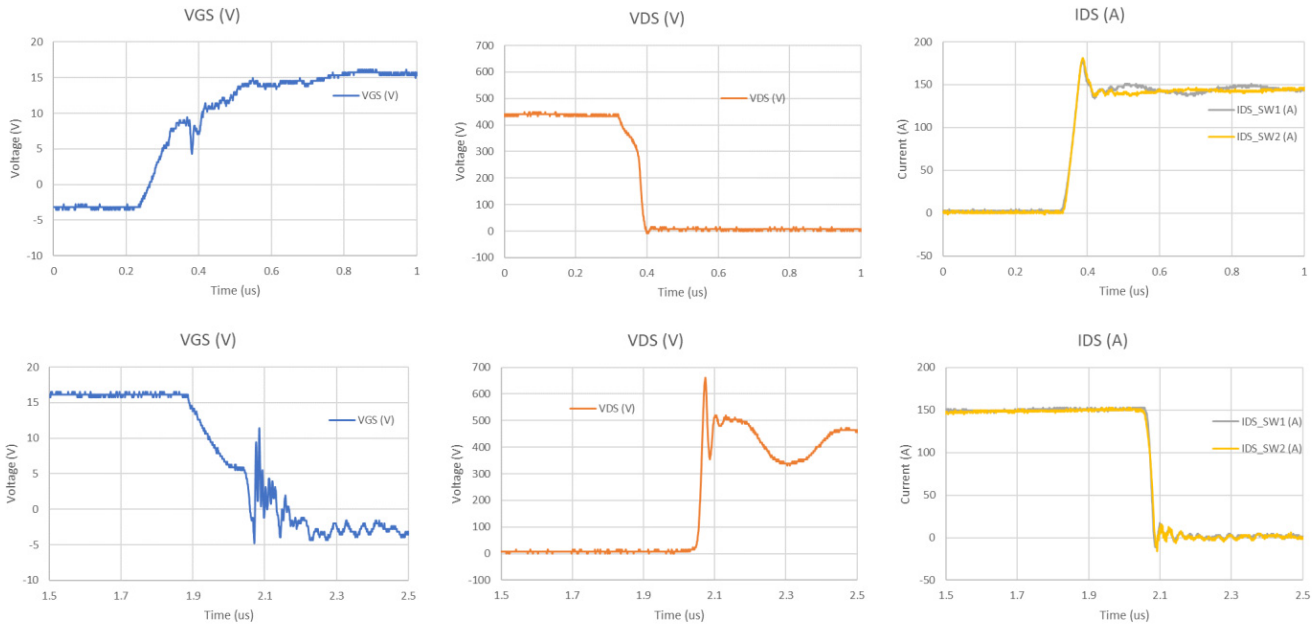

Figure 14. Waveforms of Switching – UJ4SC075006K4S

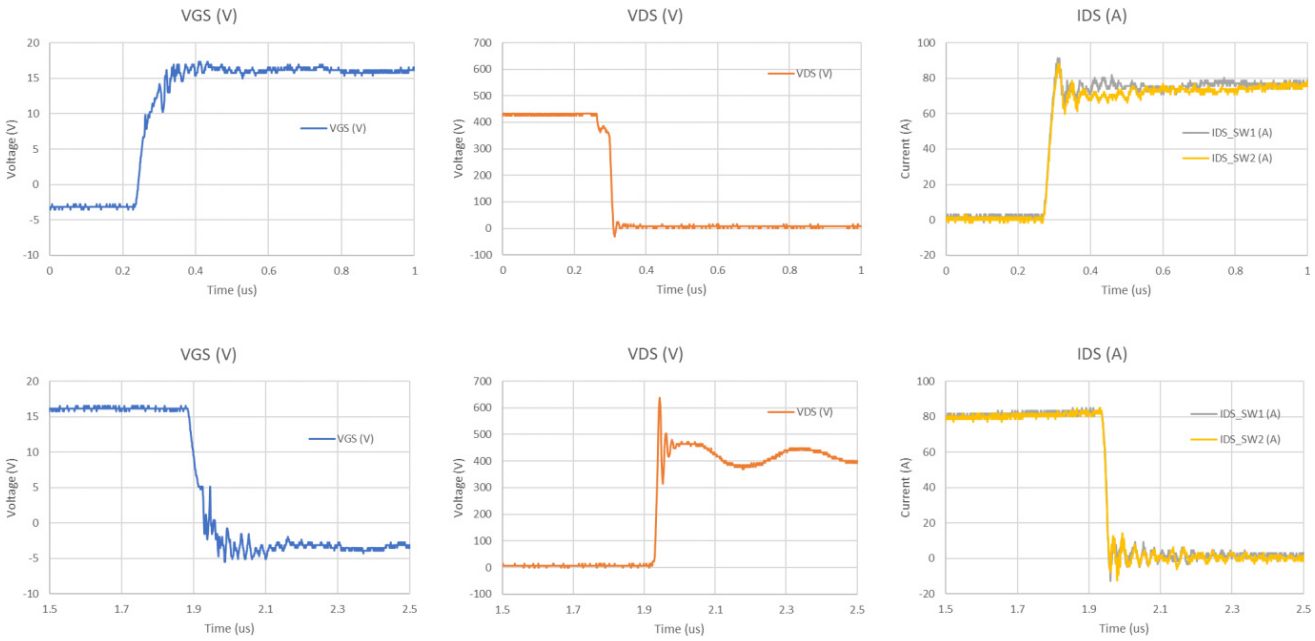

Figure 15. Waveforms of Switching – UJ4SC075006K4S

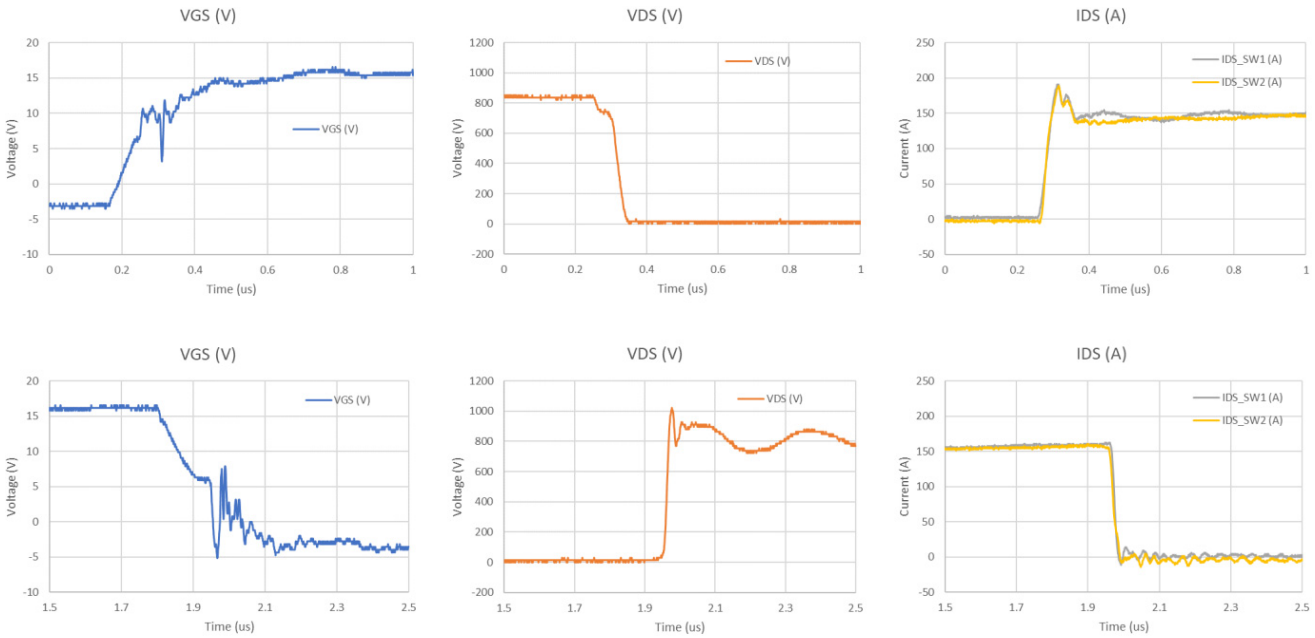

Figure 16. Waveforms of Switching – UF3SC120009K4S

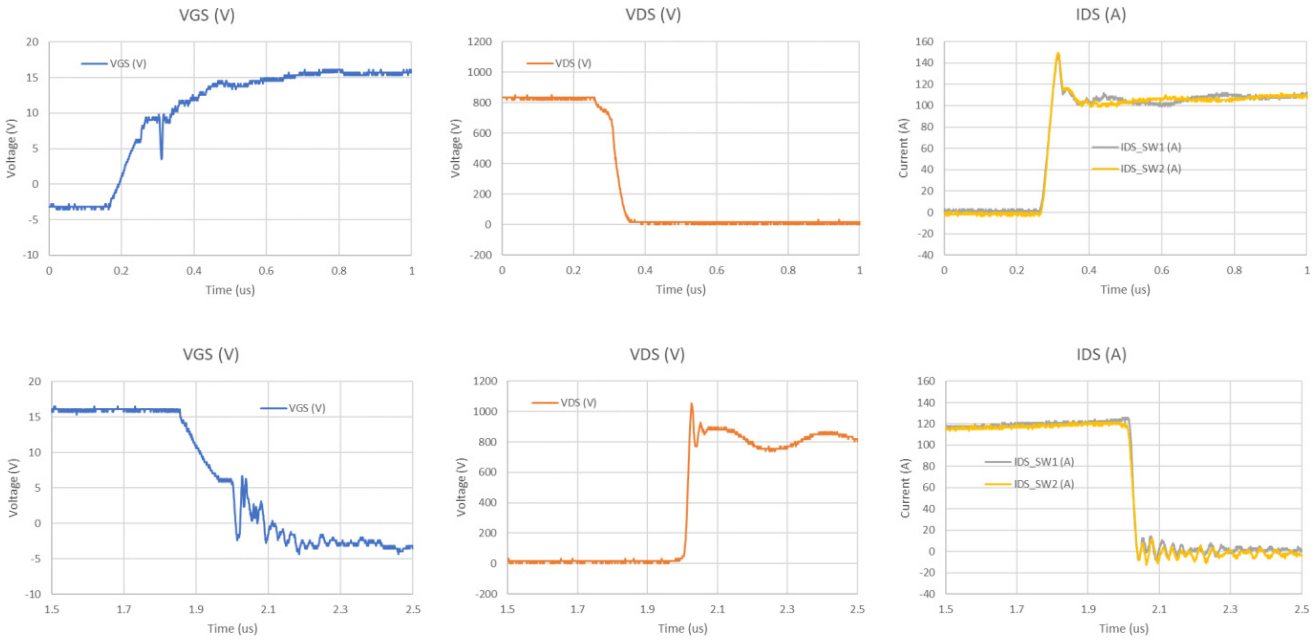

Figure 17. Waveforms of Switching – UF3SC120016K4S

Emulated Mismatch of Gate Threshold

Usually, this mismatch is unavoidable because of the difference, even slight, between real value of each device and typical value in the datasheet. Therefore, to test the effectiveness of ferrite bead and common-mode choke on gate circuit, a mismatched gate threshold level was emulated by varying the individual gate resistance (one with 6.8 Ohm and another one is 6.2 Ohm) based on UJ4SC075006K4S. Figure 18 to Figure 22 show the waveforms with different measures to mitigate the emulated unmatched gate threshold.

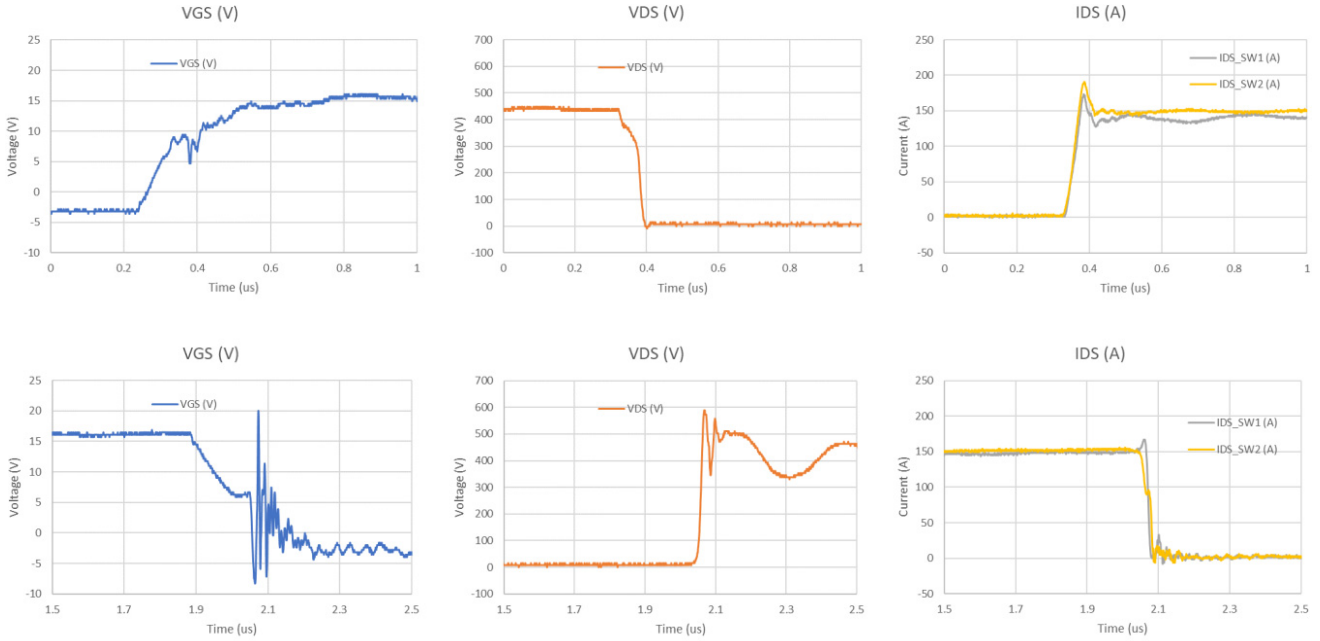

Figure 18. Varied Gate Resistance to Emulate Gate Threshold Mismatch (No Ferrite Bead)

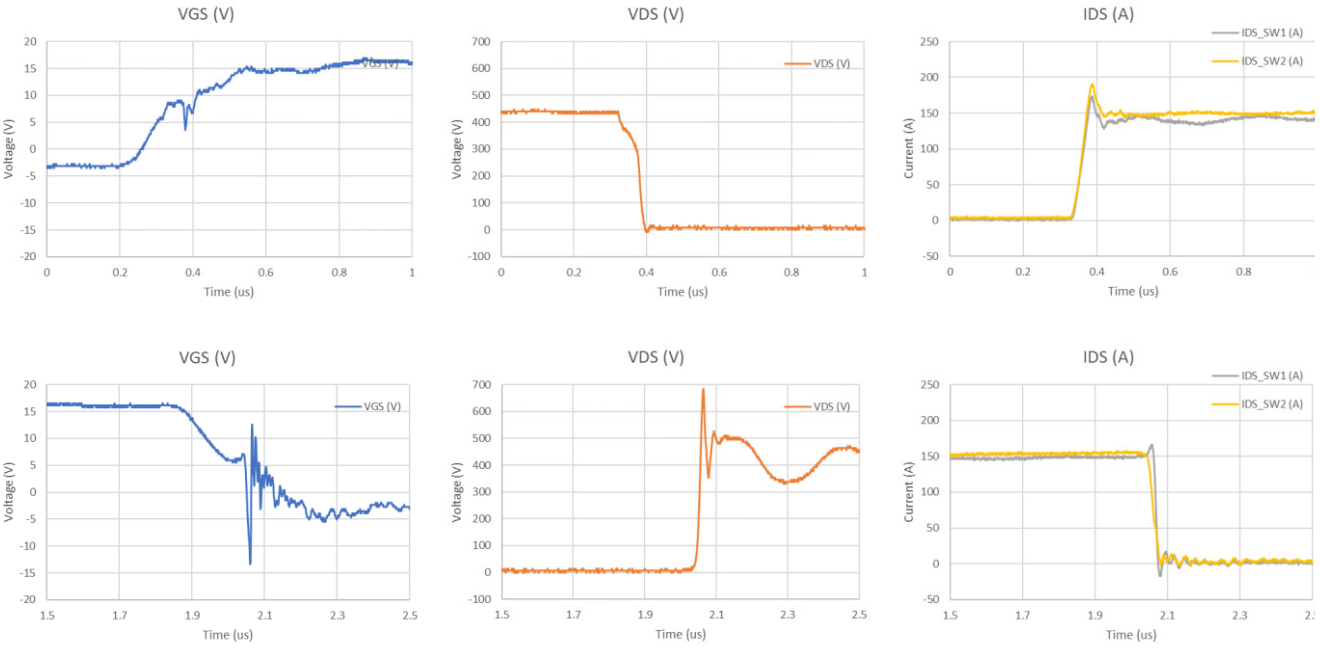

Figure 19. With Ferrite Bead on Gate

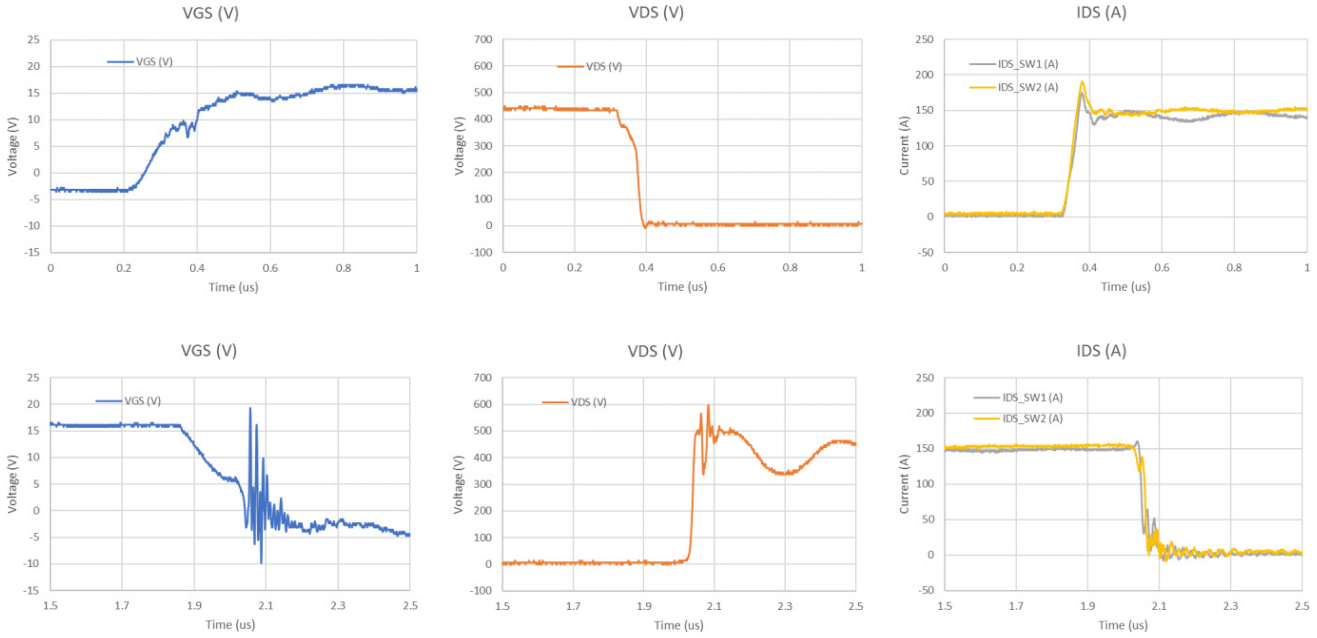

Figure 20. With Ferrite Bead on Kelvin-source

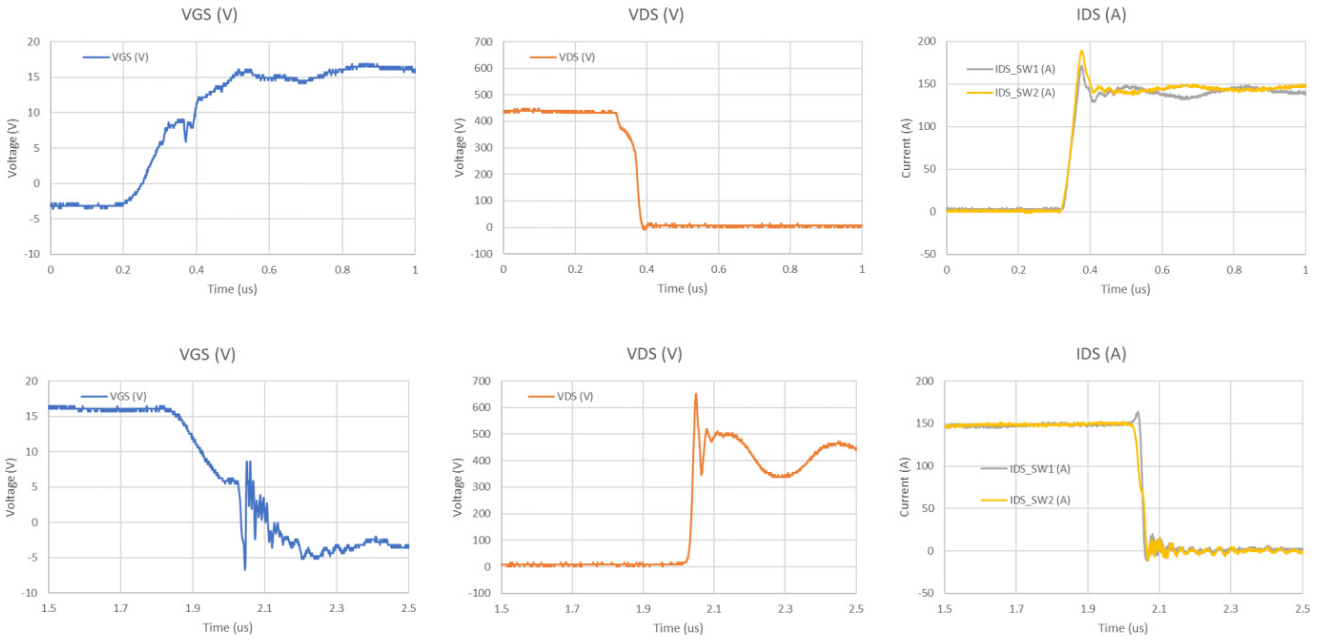

Figure 21. With Ferrite Bead on Both Gate and Kelvin-source

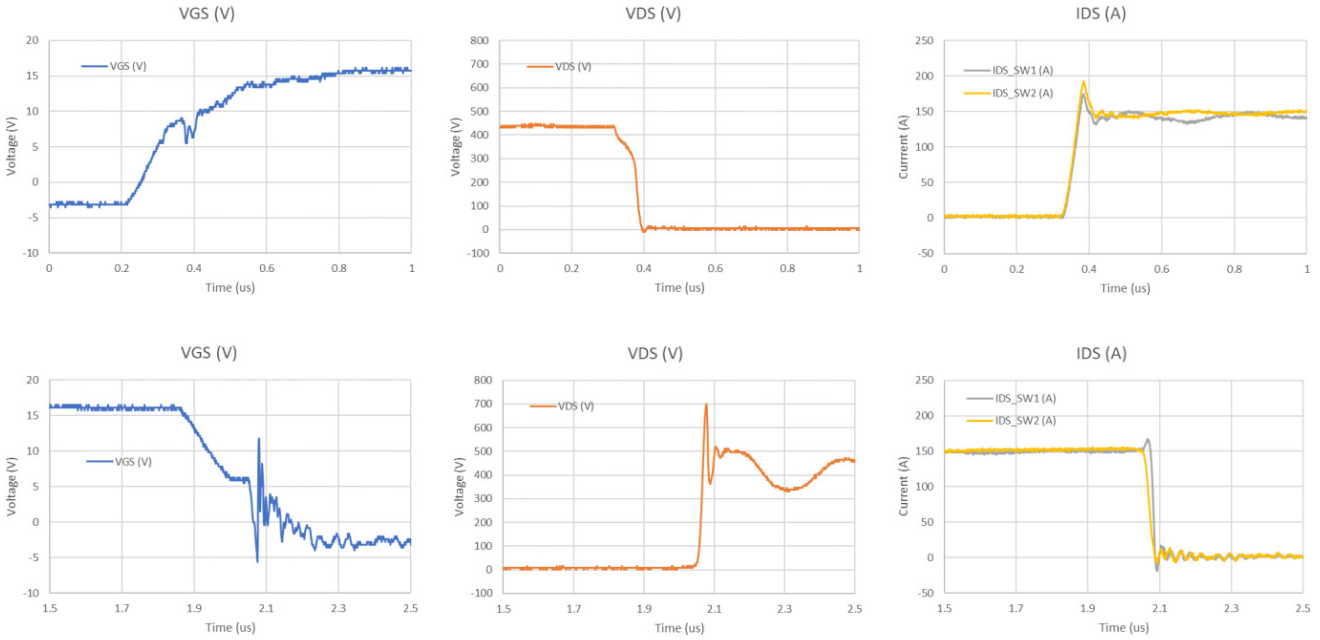

Figure 22. Common-mode Choke on Gate Circuit

From the above test results we can see, common-mode choke on gate circuit is the best way to mitigate the negative effects of V_{GS} and V_{DS}, when the devices have an unavoidable gate threshold mismatch.

Emulated Mismatch of Layout

A symmetrical layout is also an important point for paralleling devices, because asymmetrical layout will cause the difference of drain trace inductance (Ld) and source trace inductance (Ls) of different branches, which will lead to dynamic current mismatch or transient oscillation. Also, whether the position of decoupling capacitor (Cd) is symmetrical in layout is also a factor. Therefore, to test the effectiveness of ferrite bead and common-mode choke on gate circuit, a mismatched Ld/Ls of layout was emulated by varying the length of drain/source lead based on UF3SC120009K4S, and different positions of Cd in layout were compared as well. Figure 23 shows the positions of Ld, Ls and Cd. Figure 24 to Figure 28 show the waveforms with different measures to mitigate the negative influences of asymmetrical layout.

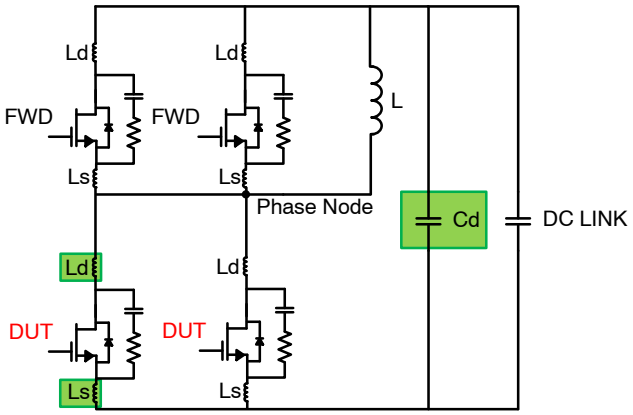

Figure 23. Positions of Ld, Ls and Cd

Figure 24. Ld Unbalance with Ferrite Bead on Both Gate and Kelvin-source (DC link 400 V, I_D = 8 A)

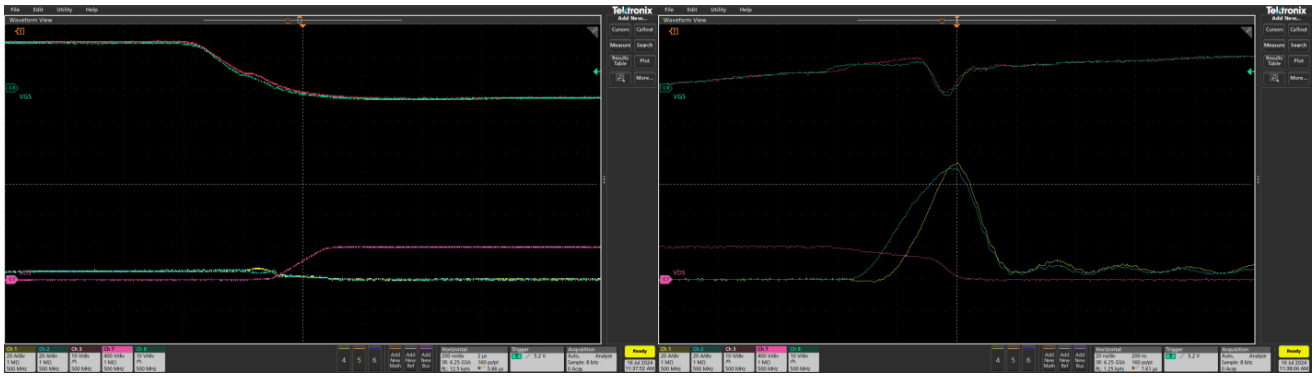

Figure 25. Ls Unbalance with Ferrite Bead on Both Gate and Kelvin-source (DC link 400 V, I_D = 6 A)

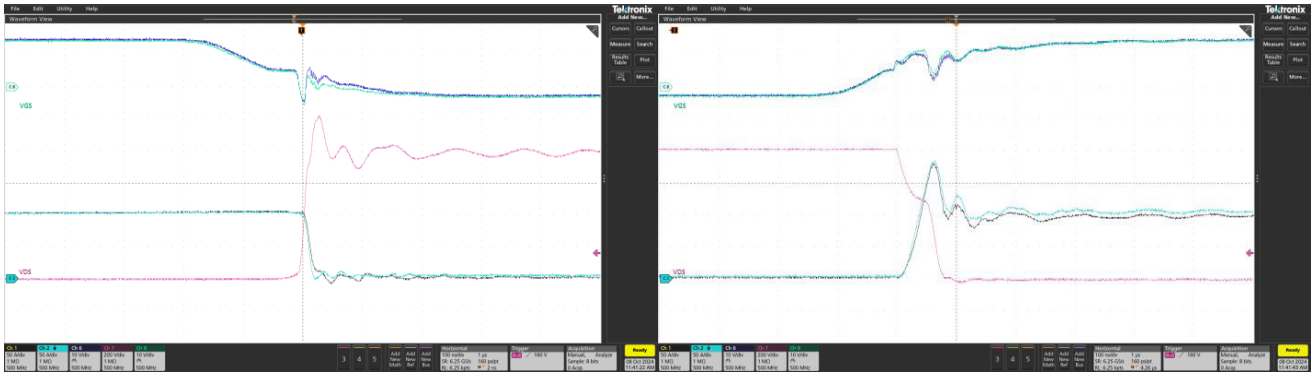

Figure 26. Asymmetrical Position of Cd with Ferrite Bead on Both Gate and Kelvin-source (DC link 800 V, I_D = 100 A)

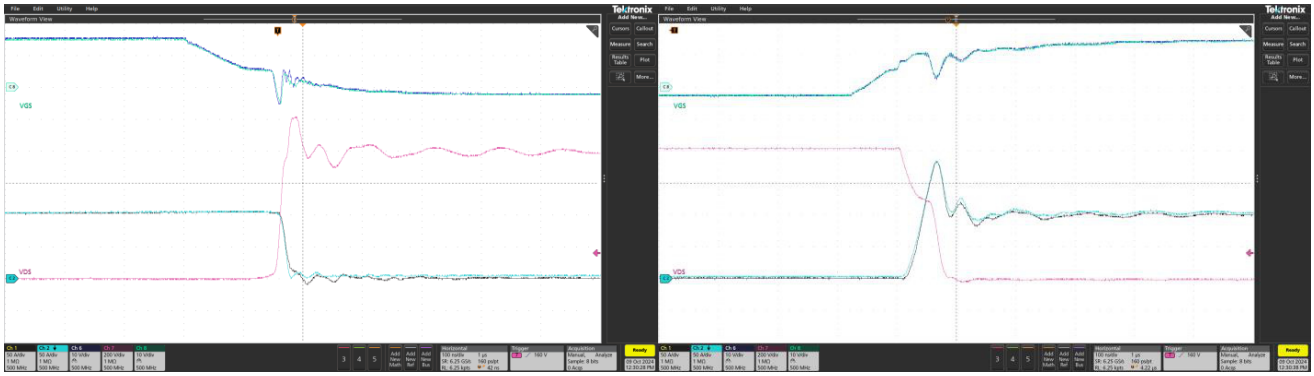

Figure 27. Asymmetrical Position of Cd with CMC on Both Gate and Kelvin-source (DC link 800 V, I_D = 100 A)

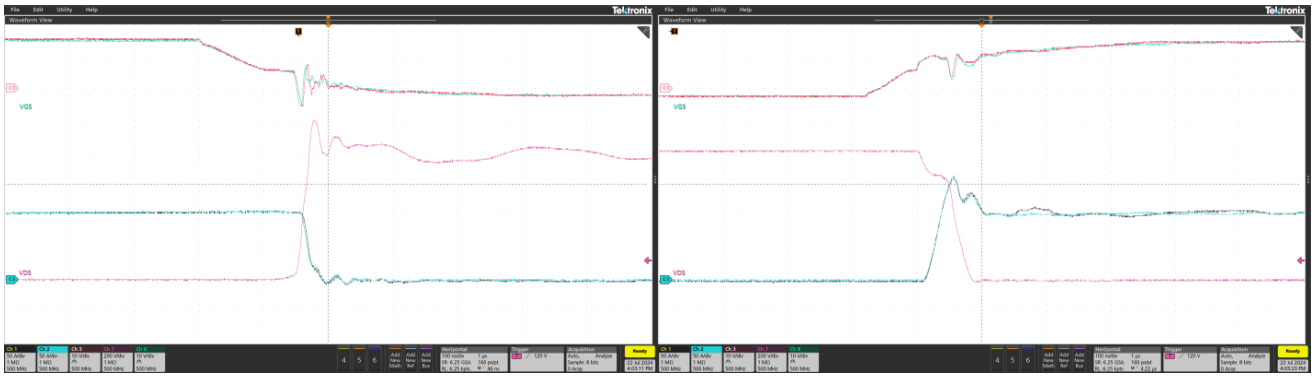

Figure 28. Symmetrical Position of Cd with CMC on Both Gate and Kelvin-source (DC Link 800 V, I_D = 100 A)

Figure 24 shows the large dynamic current mismatch caused by very unbalanced Ld. Ld-unbalance can only be solved by symmetrical layout design itself. Figure 25 shows the dynamic current mismatch caused by unbalanced Ls. We didn't set too much unbalanced Ls in this test to avoid the damage of the devices, because Ls will affect not only the power loop but also the gate loop. Ls-unbalance can be solved by the following way: making the layout design symmetrical and adding ferrite bead or common-mode choke (CMC). Adding ferrite bead can solve the Ls unbalance, but not as effective as CMC. Also, compared to CMC, ferrite bead will slow down the device and add switching loss. Therefore, we recommend to use CMC, with a symmetrical layout design for real parallel applications.

After Ld and Ls are balanced, Figure 26 shows the dynamic current mismatch caused by unbalanced Cd, still using ferrite bead in this case. Compared to Figure 26 and Figure 27, we can see that CMC on gate circuit works better than ferrite bead on balancing the current mismatch as well as the Vgs voltage. Also, again, compared to CMC, ferrite bead will slow down the device and add switching loss. But there is an important point we need to notice: CMC can only eliminate the Vgs voltage mismatch but can't eliminate the current mismatch. For the current mismatch, CMC can only mitigate it. Therefore, as Figure 28 shows, if we want to eliminate the current mismatch, the only way is placing the Cd as close and symmetrical as possible to the parallel half-bridges. Therefore, again, we recommend to use CMC, with a symmetrical layout design for real parallel applications.

Best Practices of Design and Test

- Device snubbers are required for successful paralleling of SiC FETs, showing in Figure 29. Starting values are recommended in User Guide.

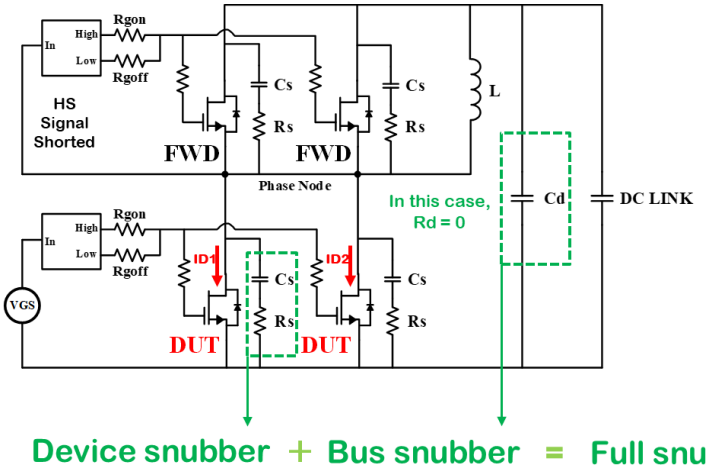

Figure 29. Device Drain-to-souce Snubber and Bus Snubber are Required for Successful Paralleling SiC FETs

- Symmetric layout is critical, it was verified by tests that the asymmetric drain & source stray inductances and the position of decoupling capacitors can cause high switching current difference.
- Common-mode choke on gate and source loop is the most effective way to eliminate the transient current mismatch or transient oscillation if the little mismatch of gate threshold and the little asymmetrical layout are unavoidable.
- Ferrite core (toroid) current transformer (CT) is not recommended because it will cause unbalanced drain stray inductance, because of the mutual inductance between lead and core. Rogowski coil current probe should be used for current measurement, shown in Figure 30.

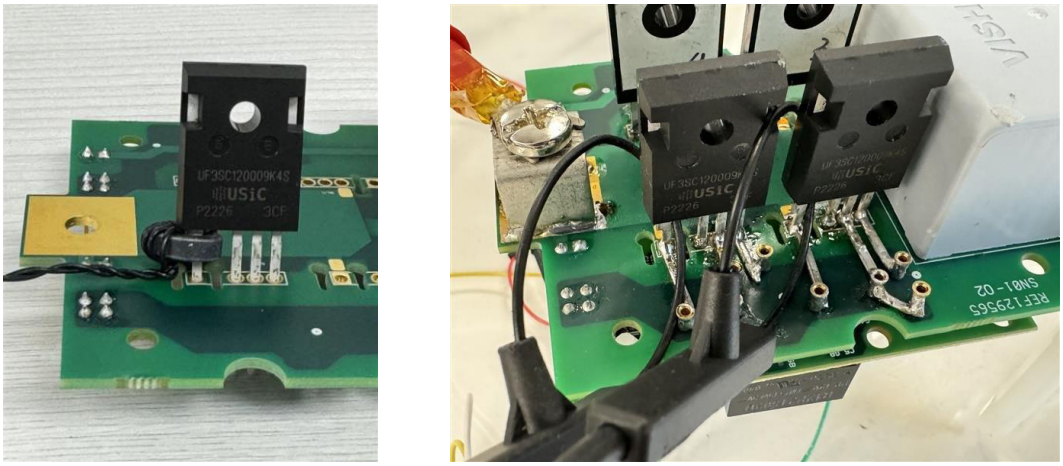

Figure 30. Current Measurement Method, Left: Ferrite Core CT (Not Recommended); Right: Rogowski Coil

- For voltage measurement, differential probe is not recommended because of its big loop of lead and wire (will add loop inductance), recommend to use passive probe with small loop inductance like shown in Figure 31.

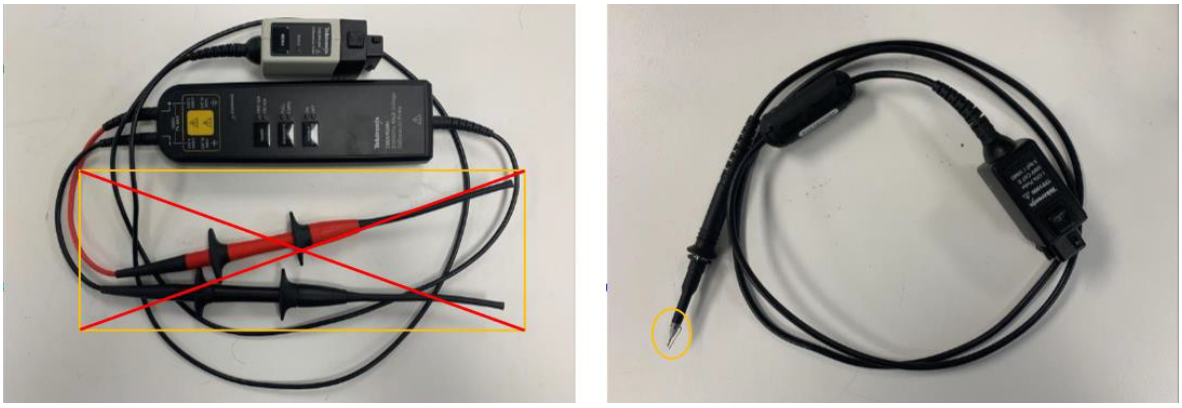

Figure 31. Voltage Probe, Left: Differential Probe (Not Recommended); Right: Passive Probe with Short Loop

- Common mode noise is easy to be coupled into the gate to source signal measurement because the high dv/dt, one way to filter out this noise is to add ferrite core on to the voltage probe cables, and twist these cables, as shown in Figure 32.

Figure 32. Filtering Common Mode Gate to Source Noise with Ferrite Core on Twisted Wires

Summary

Despite their high gain and switching slew rates, SiC JFET cascodes can be successfully paralleled by following the guidelines outlined in this application note. Although only two parallel parts were discussed, these parallel guidelines apply to any number of parallel parts. Finally, these guidelines apply not only to cascodes, but also to any other type of voltage-gated power transistors.

For applications like high power inverter which need more than two discrete in parallel, low dv/dt required and device RC snubber is not appreciated, **onsemi** recommends using the Combo-FET device.

REVISION HISTORY

Revision	Description of Changes	Date
3	Update the title and a part of the text of Chinese version on page 1. Add the revision history table.	6/4/2025

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