onsemi Smart Fuse Layout Guidelines

AND90303/D

INTRODUCTION

This document focuses on describing best practices for laying out designs utilizing NCP81428 and NCP81418 12 V Smart Fuse's, which can also be applied to other similar eFuse type devices. Following these best practices results in a better preforming solution both in terms of electrical properties and power dissipation. Not following these layout practices can lead to sub optimal performance such as negative current transients at the output and premature overheating of the device.

LAYOUT CONSIDERATIONS FOR FAVORABLE THERMAL PERFORMANCE

NCP81428 and NCP81418 are designed to dissipate heat through the EPAD (Exposed Pad) into the board they are mounted on. The board copper acts as a heatsink when these devices experience heavy loads. As such, proper layout practice must be followed to achieve the rated thermal performance of NCP81428 and NCP81418.

Exposed Pad/Board Stack up Considerations

The EPAD of NCP81428 and NCP81418 is directly connected to the drain of the internal power MOSFET. As the power MOSFET heats up due to power dissipation under heavy loads, heat is dissipated through the Smart Fuse into the Vin potential board copper. As such, the more copper weight and layers that are connected to Vin potential, specifically under the EPAD of the device, the better thermal performance is seen. It is generally recommended to allocate 6 oz − 16 oz of board copper under the EPAD for best thermal performance, see Figure 2 for example board stack−up.

Thermal Via Considerations

Thermal Via placement is another crucial factor in determining a layout's thermal performance. It is recommended to place roughly 30, 0.2 mm drill diameter/ 0.3 mm annular ring diameter, Thermal Vias in the EPAD of the device which ties the outer board copper to the inner layers. If too few Thermal Vias are used, hot spots can form on the EPAD and FET die as the thermal resistance to the inner board copper will vary in portions of the EPAD. Figure 1 shows ideal placement of in pad Thermal Vias, 33 evenly spaced 0.2 mm drill diameter/0.3 mm annular ring diameter vias are placed in the EPAD to ensure uniform thermals across the entire EPAD of the device.

The EPAD is not the only place Thermal Vias should be placed for ideal thermal performance. Placing Thermal Vias close to the Vin and Vout pins can reduce hot spots on the board close to the input and output of the Smart Fuse. Figure 1 gives an example of how this should be done properly. Notice that the Vias are evenly distributed in the Vin and Vout power plane just as how they are in the EPAD.

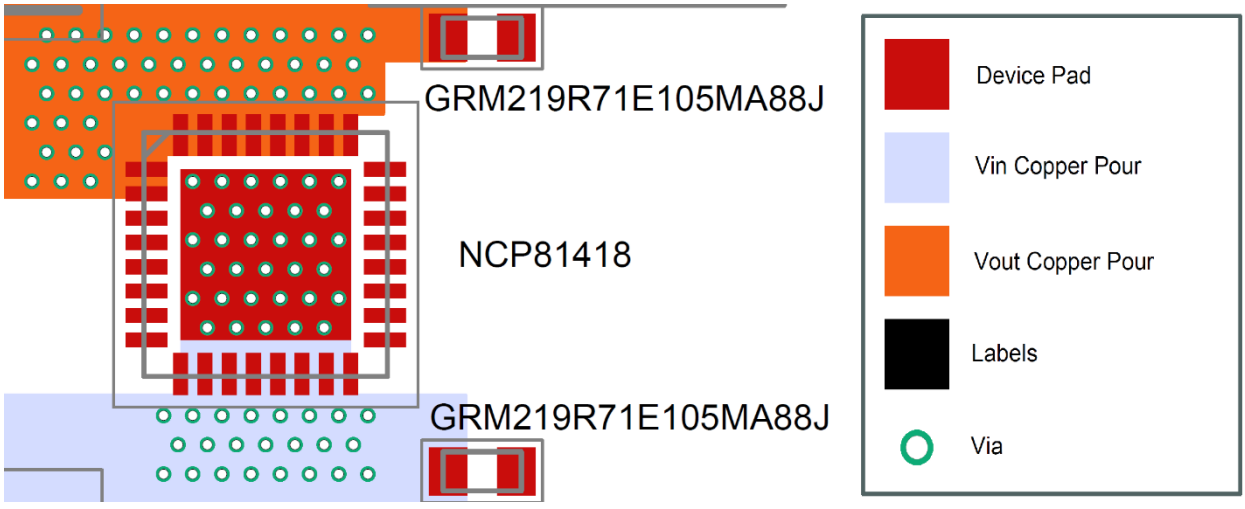

Figure 1. Example NCP81418 Device Layout with 0.2mm Drill Diameter, 0.3 mm Annular Ring Diameter Vias

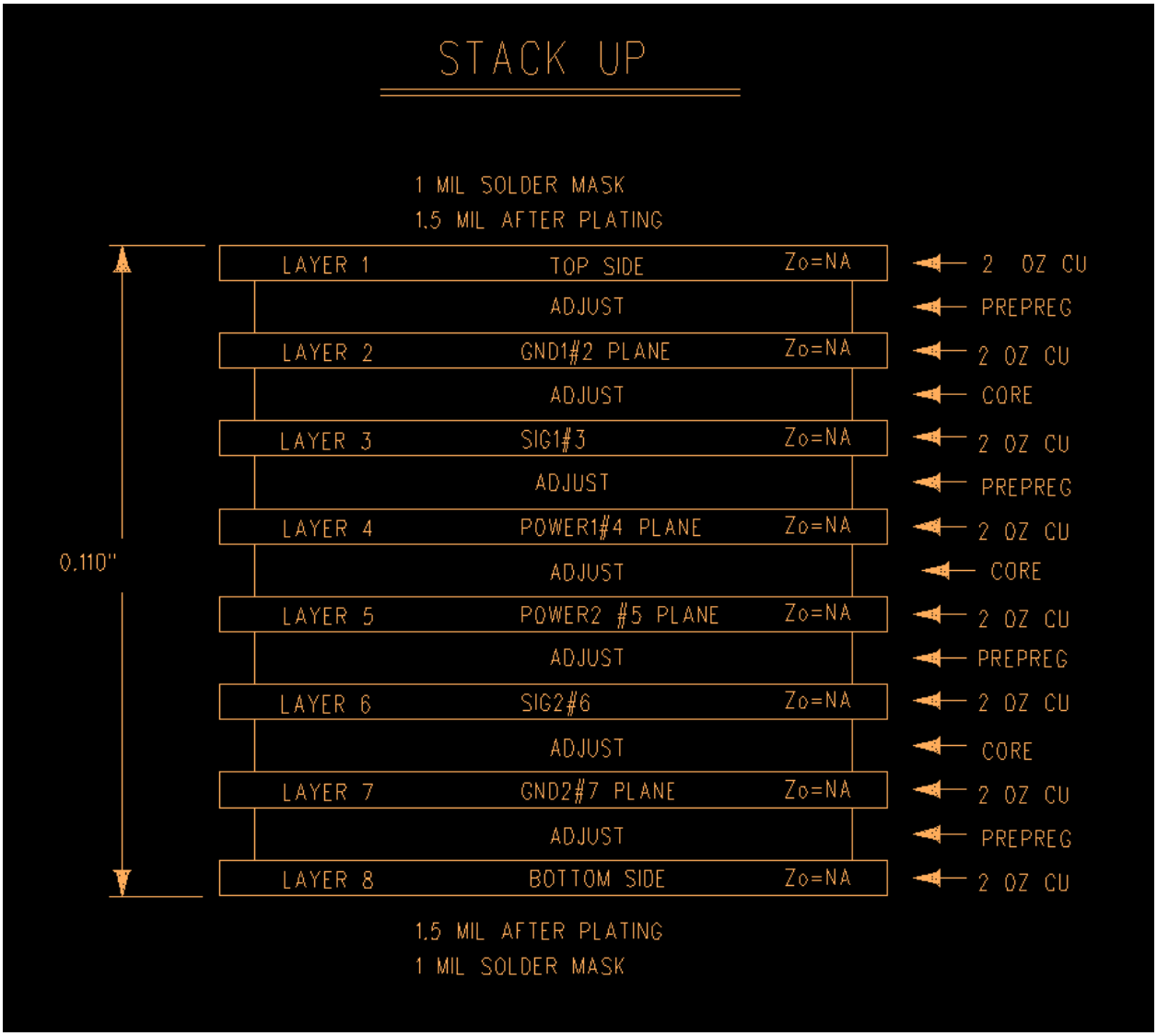

Figure 2. NCP81428/NCP81418 Example Board Stack−up

LAYOUT CONSIDERATIONS TO MINIMIZE EFFECTS OF PARASITIC POWER PLANE INDUCTANCE AND TRANSIENTS

NCP81428 and NCP81418, just as other similar eFuse devices, require special layout consideration to avoid potential positive voltage transients at Vin and negative voltage transients at Vout. Eliminating the possibility of these transients can be done through proper protection diode and capacitor placement.

Mitigating Positive Input Voltage Transients

Positive voltage transients can occur on the input of the Smart Fuse due to rapidly changing load conditions. When an OCP event occurs or similar high load to zero load event, the voltage at Vin of the Smart Fuse spikes because the power supply connected to Vin takes time to react to the new load conditions. If this voltage spike is large enough it can permanently damage the NCP81428 and NCP81418. To prevent this voltage spike it is recommended to place one SMBJ13A or similar 600 W peak pulse power TVS diode per phase as close to the input of the Smart Fuse as possible, see Figure 3. This TVS along with a 220 μF to 1 mF electrolytic capacitor placed as close to the input of the Smart Fuse as possible allow for complete protection against input voltage transients.

Mitigative Negative Output Voltage Transients

Negative voltage transients can occur on the output of the Smart Fuse due to rapid negative load transients when proper precaution is not taken. All designs have some amount of parasitic inductance in their power plane. When a current load rapidly goes from a high load to a close to zero−amp load, the parasitic inductance can cause the output voltage of the Smart Fuse to temporarily drop negative. To prevent this, a Schottky rectifier, such as MBR2045MFST1G, as recommended in the NCP81428 and NCP81418 Data Sheet, should be placed as close to the Vout pins of the Smart Fuse as possible. A single

MBR2045MFST1G should be used from one to three phase applications while two MBR2045MFST1G should be used from four to seven phase applications. Additionally, placing a 220 μF to 1 mF electrolytic capacitor as close to the Smart Fuse output as possible allows a source for current draw in the event of large negative slope load transients. The rectifier is placed for extreme cases where just the capacitor is not enough to prevent the negative voltage transient. It can also be helpful to place a large input filtering capacitor as close to the device drawing the current load as possible to further reduce the possibility of negative voltage transients.

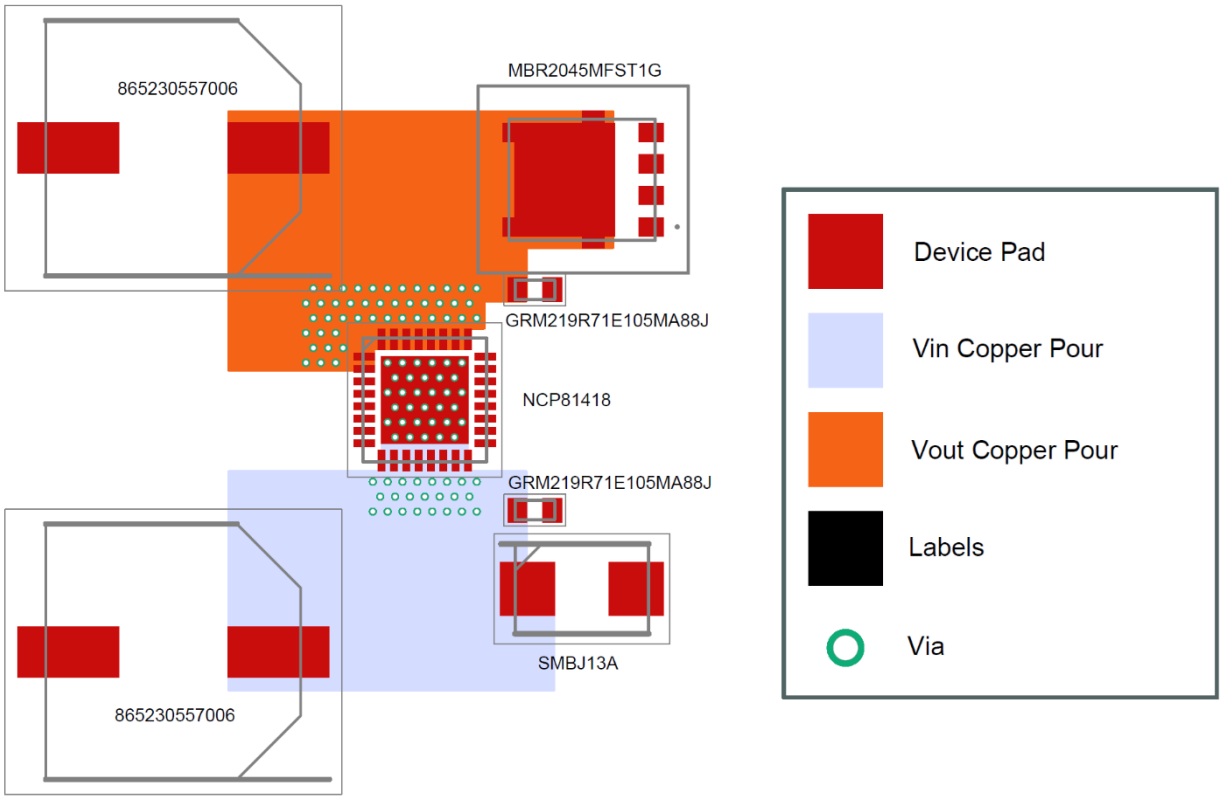

Figure 3. Example Diode and Capacitor Placement

SUMMARY

Using the layout practices described in this document will allow NCP81428/NCP81418 to operate as intended in the system they are implemented in. Failure to layout these devices properly can lead to unpredictable performance or even damage to the Smart Fuse devices.

ADDITIONAL INFORMATION

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