3-phase Inverter Power Module 1200 V SPM® 31 Version 2 Series Application Note

AND90262/D

INTRODUCTION

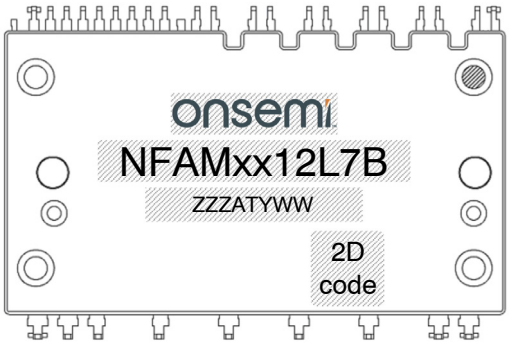
This application note provides practical guidelines for designing with the SPM 31 version 2 Series power modules.

This series of Intelligent Power Modules (IPM) for 3-phase motor drives contains a three-phase inverter stage, gate drivers.

Design Concept

The SPM 31 version 2 design objective is to provide a minimized package and a low power consumption module with improved reliability. It is achieved by applying new gate-driving High-Voltage Integrated Circuit (HVIC), a new Insulated-Gate Bipolar Transistor (IGBT) of advanced silicon technology and improved Direct Bonded Copper (DBC) substrate based on transfer mold package. The SPM 31 version 2 achieves reduced board size and improved reliability compared to existing discrete solutions. Target applications are inverter motor drives for industrial use, such as commercial air conditioners, general-purpose inverters and servo motors. The temperature sensing function of SPM 31 version 2 products are implemented in the LVIC to enhance the system reliability. The analog voltage proportional to the temperature of the LVIC in module is provided for monitoring the module temperature and necessary protections against over−temperature situations. Figure 1 shows the package outline structure.

MARKING DIAGRAM



onsemi Logo
NFAMxx12L7B = Specific Device Code
ZZZ = Assembly Lot Code
A = Assembly Location
T = Test Location
Y = Year
WW = Work Week
2D Code
Device marking is on package top side

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packaging)
NFAMxx12L7B	DIP39, 31.0 x 54.5	90 / BOX

Figure 1. External View and Internal Structure of SPM 31 Version 2

Key Features

- 1200 V / 15, 25, 35 A, three phase FS7 IGBT inverter including control ICs for gate driving and protections
- Very low thermal resistance by adopting DBC substrate
- Easy PCB layout thanks to built−in bootstrap circuits
- Open emitter configuration for easy monitoring of each phase current sensing
- Single-grounded power supply thanks to built−in HVICs and bootstrap operations
- Built-in temperature sensing function by LVIC
- Isolation Rating of 2500 Vrms / min.

PRODUCT DESCRIPTION

Ordering Information

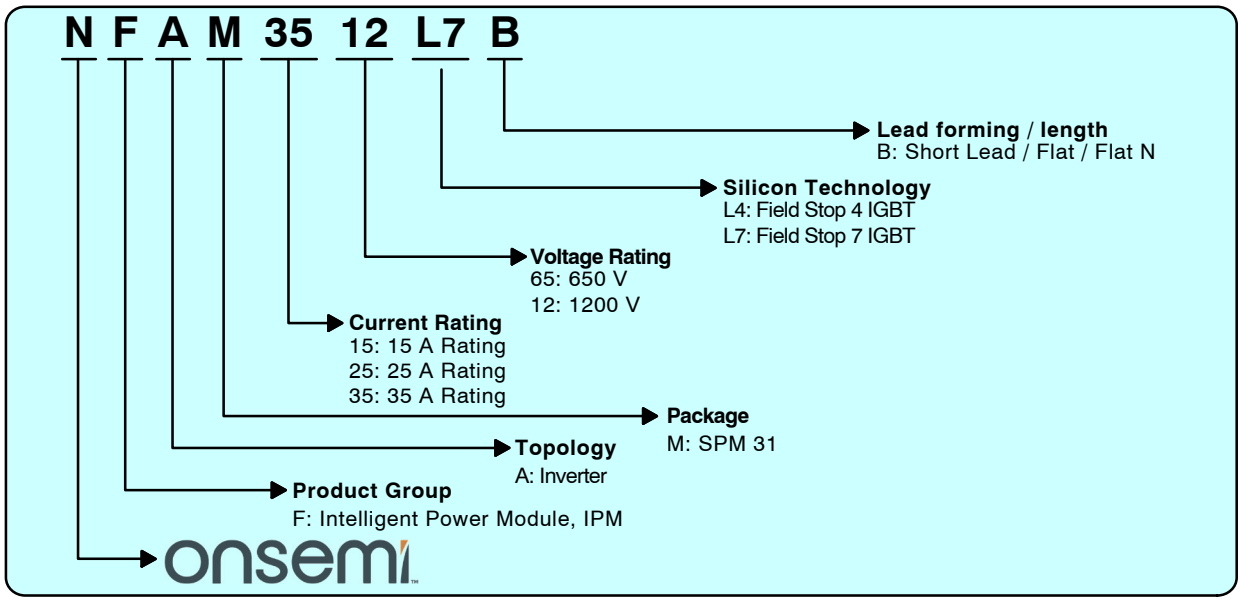


Figure 2. Ordering Information

Product Line−up

Table 1 shows the SPM31 version 2 product line up without package variations. Online simulation tool, Motion Control Design Tool (Click for simulation tool) is recommended to find out the right product for the desired application. For package drawing, please refer to Chapter Package Outline.

Table 1. PRODUCT LINE−UP

Product	Current/Voltage	Recommend Power (Note 1)	Target Application	Isolation Voltage
NFAM1512L7B	15 A / 1200 V	2.0 kW	Air Conditioners, Industrial motors, General−purpose inverters, Servo motors	V_{ISO} = 2500 V_{RMS} (Sine 60 Hz, 1−min All Shorted Pins Heat Sink)
NFAM2512L7B	25 A / 1200 V	3.5 kW		
NFAM3512L7B	35 A / 1200 V	5.0 kW		
NFAM4012L7B (Note 2)	40 A / 1200 V	6.0 kW		

1. These power ratings are simulated result by specific operating conditions, so it can be changed by the operating conditions.
2. Under development.

Internal Circuit Diagram

Three bootstrap circuits generate the voltage needed for driving the high-side IGBTs. The bootstrap diodes are internal part in HVIC and driving voltage of high−side IGBTs is sourced from VDD (15 V) through bootstrap circuits. There is an internal level shift circuit for the high−side drive signals allowing all control signals to be driven directly from GND levels common with the control circuit such as the microcontroller without requiring external isolation with opto−couplers. LVIC temperature sensing signal is output from the VTS pin.

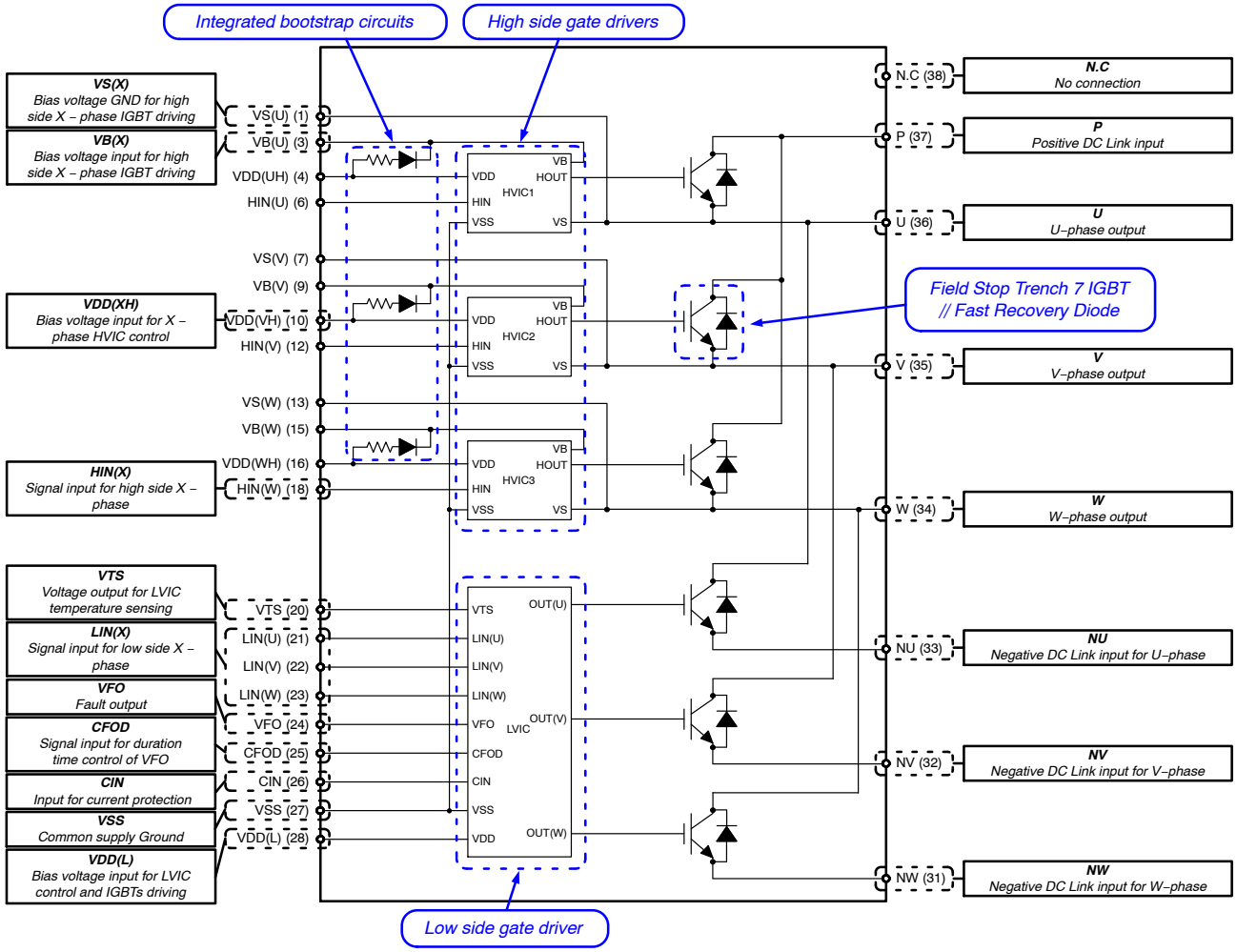


Figure 3. Internal Equivalent Circuit Diagram

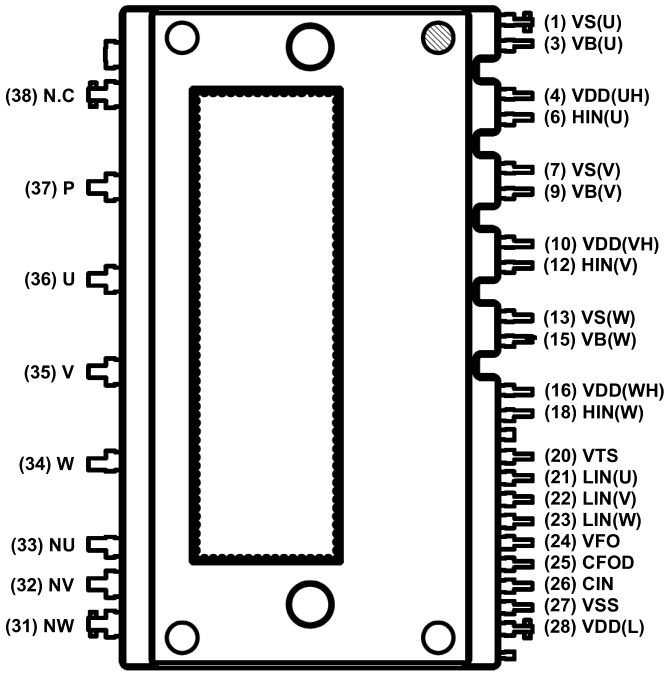


Figure 4. Package Top–View and Pin Assignment

Table 2. NUMBERS, NAMES AND DUMMY PINS

Pin Number	Name	Description
1	VS(U)	High−Side Bias Voltage GND for U Phase IGBT Driving
(2)	−	Dummy
3	VB(U)	High−Side Bias Voltage for U Phase IGBT Driving
4	VDD(UH)	High−Side Bias Voltage for U Phase IC
(5)	−	Dummy
6	HIN(U)	Signal Input for High−Side U Phase
7	VS(V)	High−Side Bias Voltage GND for V Phase IGBT Driving
(8)	−	Dummy
9	VB(V)	High−Side Bias Voltage for V Phase IGBT Driving
10	VDD(VH)	High−Side Bias Voltage for V Phase IC
(11)	−	Dummy
12	HIN(V)	Signal Input for High−Side V Phase
13	VS(W)	High−Side Bias Voltage GND for W Phase IGBT Driving
(14)	−	Dummy
15	VB(W)	High−Side Bias Voltage for W Phase IGBT Driving
16	VDD(WH)	High−Side Bias Voltage for W Phase IC
(17)	−	Dummy
18	HIN(W)	Signal Input for High−Side W Phase
(19)	−	Dummy
20	VTS	Voltage Output for LVIC Temperature Sensing Unit
21	LIN(U)	Signal Input for Low−Side U Phase
22	LIN(V)	Signal Input for Low−Side V Phase
23	LIN(W)	Signal Input for Low−Side W Phase
24	VFO	Fault Output
25	CFOD	Capacitor for Fault Output Duration Selection
26	CIN	Input for Over Current Protection
27	VSS	Low−Side Common Supply Ground
28	VDD(L)	Low−Side Bias Voltage for IC and IGBTs Driving
(29)	−	Dummy
(30)	−	Dummy
31	NW	Negative DC−Link Input for W Phase
32	NV	Negative DC−Link Input for V Phase
33	NU	Negative DC−Link Input for U Phase
34	W	Output for W Phase
35	V	Output for V Phase
36	U	Output for U Phase
37	P	Positive DC−Link Input
38	N.C	No Connection
39	−	Dummy

3. Pins of ( ) are the dummy for internal connection. These pins should be no connection.

Detailed Pin Definition and Notification

Pins: VB(U)−VS(U), VB(V)−VS(V), VB(W)−VS(W)

- High-side bias voltage pins for driving the IGBTs and high-side bias voltage ground pins for driving the IGBTs.
- VB(U), VB(V), VB(W) pins are connected to cathode pins of bootstrap diodes on each phase.
- These are drive power supply pins for providing gate drive power to the high-side IGBTs.
- The virtue of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high-side IGBTs.
- Each bootstrap capacitor is charged from the VDD supply during ON state of the corresponding low-side IGBTs and Diodes.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low-ESR, low-ESL) filter capacitor should be mounted very close to these pins.

Pins: VDD(L), VDD(UH), VDD(VH), VDD(WH)

- Low-side and high-side bias voltage pins.
- These are control supply pins for the built-in ICs.
- These four pins should be connected externally.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low-ESR, low-ESL) filter capacitor should be mounted very close to these pins.

Pin: VSS

- Common supply ground pin.
- This is supply ground pin for the built−in ICs.
- Important! To avoid noise influences, the main power circuit current should not be allowed to blow through this pin.

Pins: HIN(U/V/W), LIN(U/V/W)

- Signal input pins.
- These pins control the operation of the built-in IGBTs.
- They are activated by voltage input signals. The terminals are internally connected to a Schmitt-trigger circuit composed of 5 V-class CMOS.
- The signal logic of these pins is active high. The IGBT associated with each of these pins is turned ON when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the SPM 31 version 2 products against noise influences.
- To prevent signal oscillations, an RC coupling as illustrated in Figure 22 is recommended.

Pin: CIN

- Over−current and short−circuit detection input pin.
- The current sensing shunt resistor should be connected between the low-pass filter before the CIN pin and the low-side ground pin VSS to detect over or short circuit current.
- The shunt resistor should be selected to meet the detection levels matched for the specific application.
- An RC filter should be connected to the CIN pin to eliminate noise.
- The connection length between the shunt resistor and CIN pin should be minimized.

Pin: VFO

- Fault output pin.
- This is the fault output alarm pin. An active low output is given on this pin for a fault state condition in the SPM 31 version 2 products.
- The alarm conditions are Over−Current Protection (OCP), or low-side bias Under-Voltage Lock Out (UVLO) operation.

- The VFO output is open drain configured. The VFO signal line should be pulled up to the 5 V logic power supply with approximately 10 kΩ resistance.

Pin: CFOD

- Input pin for duration time control of fault−out
- The duration time of fault-out depends on the capacitance between CFOD and VSS pins.

Pin: VTS

- Analog temperature sensing output pin.
- This is to indicate the temperature of LVIC with analog voltage. LVIC itself creates some power loss, but mainly heat generated from the IGBTs will increase the temperature of the LVIC.
- VTS versus temperature characteristics is illustrated in Figure 15.

Pin: P

- Positive DC−link pin.
- This is the DC−link positive power supply pin of the inverter.
- It is internally connected to the collectors of the high-side IGBTs.
- To suppress surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (tip: metal film capacitor is typically used).

Pins: NU, NV, NW

- Negative DC-link pins.
- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low-side IGBT emitters of each phase.
- These pins are used to connect one shunt resistor or three shunt resistors for current sensing.

Pins: U, V, W

- Inverter power output pins.
- Inverter output pins for connecting to the inverter load (e.g. motor).

PACKAGE

Package Structure

Since heat dissipation is an important factor limiting the power module's current capability, the heat dissipation characteristics of a package are important in determining the performance. A trade−off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to a good package technology lies in the optimization package size while maintaining outstanding heat dissipation characteristics without compromising the isolation rating.

In SPM 31 version 2, technology was developed with DBC substrate that resulted in excellent heat dissipation characteristics. This technology made it possible to achieve improved reliability and heat dissipation. Power chips are attached directly to the DBC substrate.

Figure 5 and Figure 6 show the package outline and the cross−sections of the SPM 31 version 2 package.

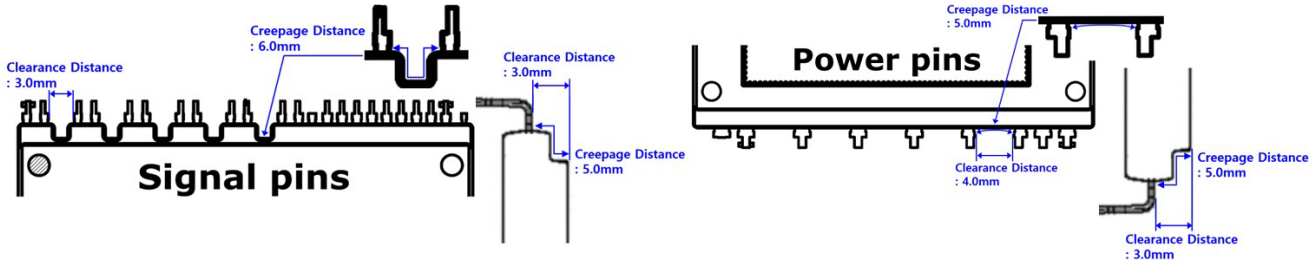


Figure 5. Isolation Distance for Signal Pins, Power Pins and Pins to Heatsink

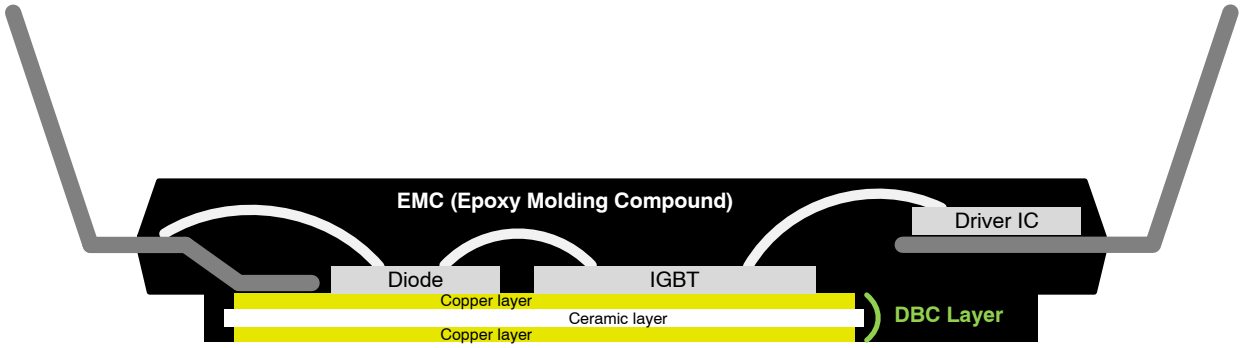
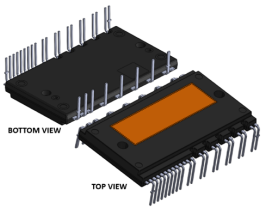


Figure 6. Package Structure and Cross Section for SPM 31 Version 2

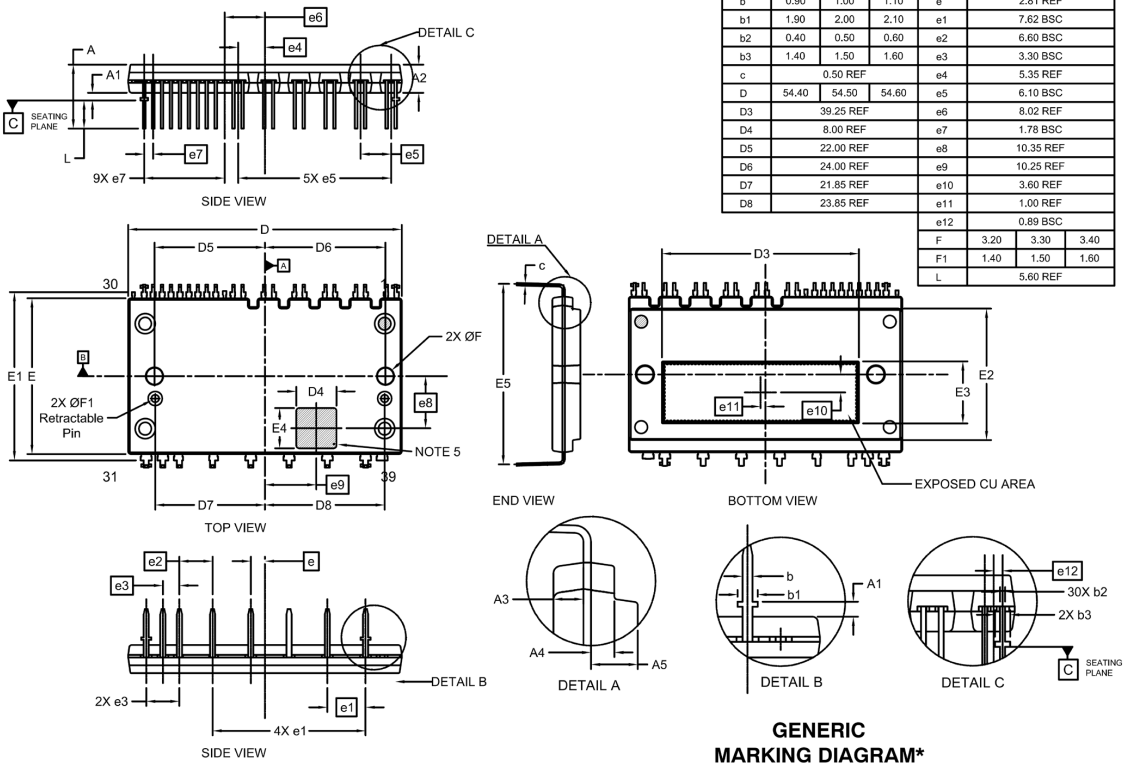
Package Outline



DIP39, 54.5x31.0 EP−2
CASE MODGX
ISSUE O

DATE 02 APR 2019

DIM	MILLIMETERS MIN.	NOM.	MAX.	DIM	MILLIMETERS MIN.	NOM.	MAX.
A	12.20	12.7	13.2	E	30.90	31.00	31.10
A1	1.00	1.50	2.00	E1	33.50 REF		
A2	5.50	5.60	5.70	E2	26.14 REF		
A3	2.00 REF			E3	12.35 REF		
A4	1.55 REF			E4	8.00 REF		
A5	3.10 REF			E5	35.40	35.90	36.40
b	0.90	1.00	1.10	e	2.81 REF		
b1	1.90	2.00	2.10	e1	7.62 BSC		
b2	0.40	0.50	0.60	e2	6.60 BSC		
b3	1.40	1.50	1.60	e3	3.30 BSC		
c	0.50 REF			e4	5.35 REF		
D	54.40	54.50	54.60	e5	6.10 BSC		
D3	39.25 REF			e6	8.02 REF		
D4	8.00 REF			e7	1.78 BSC		
D5	22.00 REF			e8	10.35 REF		
D6	24.00 REF			e9	10.25 REF		
D7	21.85 REF			e10	3.60 REF		
D8	23.85 REF			e11	1.00 REF		
				e12	0.89 BSC		
				F	3.20	3.30	3.40
				F1	1.40	1.50	1.60
				L	5.60 REF		



NOTES:
1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b and c APPLY TO THE PLATED LEADS AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP.
4. POSITION OF THE LEAD IS DETERMINED AT THE BASE OF THE LEAD WHERE IT EXITS THE PACKAGE BODY.
5. AREA FOR 2D BAR CODE.
6. SHORTENED/CUT PINS ARE 2,5,8,11,14,17,19,29, 30 AND 39.

GENERIC MARKING DIAGRAM*

XXXXXXXXXXXXXXXXX
ZZZATYWW

XXXXX = Specific Device Code
ZZZ = Assembly Lot Code
AT = Assembly & Test Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON05290H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DIP39, 54.5x31.0 EP−2**	**PAGE 1 OF 1**

Figure 7. Package Outline

7PRODUCT SYNOPSIS

Absolute maximum ratings, electric characteristics, recommended operating conditions and mechanical characteristics are focused on in this section. Please refer to respective datasheets for the detailed description of each product.

ABSOLUTE MAXIMUM RATINGS (Tj = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Rating	Unit
INVERTER PART (BASE ON NFAM3512L7B)				
VPN	Supply Voltage	Applied between P – NU, NV, NW	900	V
VPN(surge)	Supply Voltage (Surge)	Applied between P – NU, NV, NW (Note 4)	1000	
Vces	Collector - Emitter Voltage		1200	
±Ic	Each IGBT Collector Current	Tc = 25 °C, Tj ≤ 150°C	35	A
±Icp	Each IGBT Collector Current (Peak)	Tc = 25°C, Tj ≤ 150°C, Under 1 ms Pulse Width	70	
Pc	Collector Dissipation	Tc = 25°C per One Chip (Note 5)	167	W
Tj	Operating Junction Temperature		–40~150	°C
CONTROL PART				
VDD	Control Supply Voltage	Applied between VDD(XX) – VSS	20	V
VBS	High-Side Control Bias Voltage	Applied between VB(X) – VS(X)	20	
VIN	Input Signal Voltage	Applied between HIN(X), LIN(X) – VSS	–0.3~V_{DD} + 0.3	
VFO	Fault Output Supply Voltage	Applied between VFO – VSS	–0.3~V_{DD} + 0.3	
IFO	Fault Output Current	Sink Current at VFO Pin	2	mA
VCIN	Current Sensing Input Voltage	Applied between CIN – VSS	–0.3~V_{DD} + 0.3	V
BOOTSTRAP DIODE PART				
VRRM	Maximum Repetitive Reverse Voltage		1200	V
Tj	Operating Junction Temperature		–40~150	°C
TOTAL SYSTEM				
VPN(PROT)	Self–Protection Supply Voltage Limit (Short–Circuit Protection Capability)	VDD(XX), VB(X) = 13.5~16.5 V, Tj = 150°C, (Non–Repetitive, <2 μs)	800	V
Tc	Case Operation Temperature	See Figure 8	–40~125	°C
Tstg	Storage Temperature		–40~125	
Viso	Isolation Voltage	60 Hz, Sinusoidal, 1–minute, Connect Pins to Heat Sink	2500	Vrms

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. Surge voltage developed by the switching operation due to the wiring inductance between P and NU, NV, NW terminals.
5. Calculation value considered to design factor.

THERMAL RESISTANCE (Tj = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Rth(j–c)Q	Junction to Case Thermal Resistance (Note 6)	Inverter IGBT Part (per 1/6 Module)	–	–	0.75	°C/W
Rth(j–c)F		Inverter FWDi Part (per 1/6 Module)	–	–	1.00	

6. For the measurement point of case temperature (Tc), please refer to Figure 8.

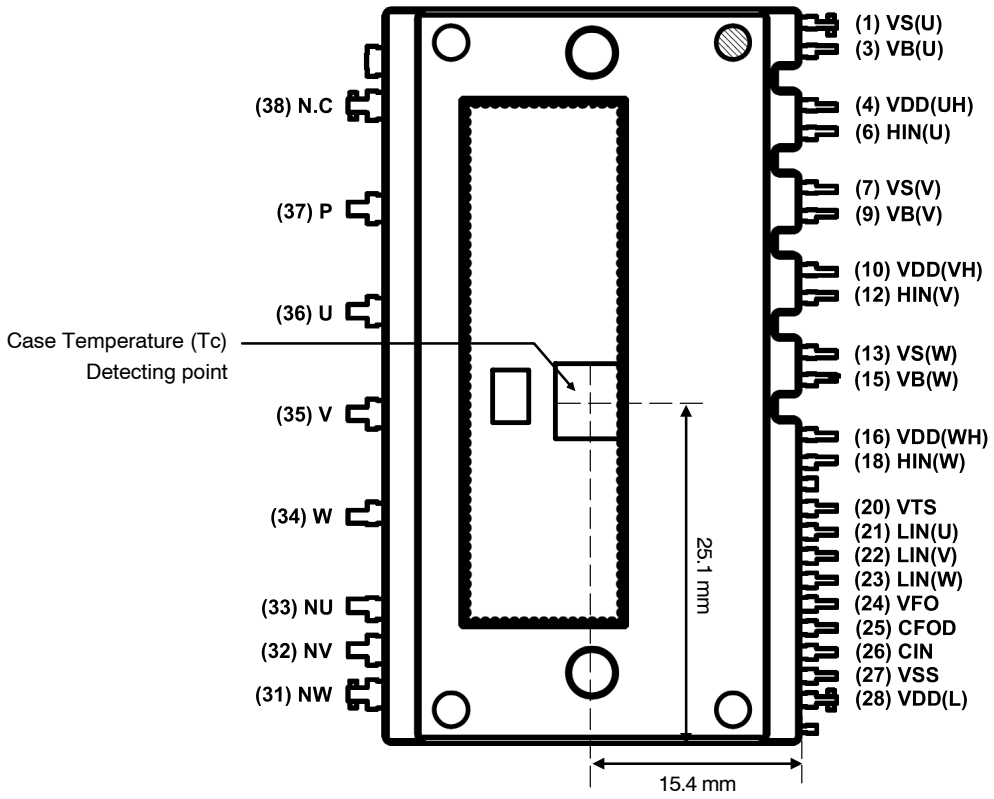


Figure 8. Case Temperature (Tc) Detecting Point

ELECTRICAL CHARACTERISTICS (VDD = 15 V and Tj = 25°C unless otherwise noted)

Symbol		Parameter	Condition	Min	Typ	Max	Unit
INVERTER PART (BASE ON NFAM3512L7B)							
VCE(sat)		Collector – Emitter Saturation Voltage	VDD = VBS = 15 V, Ic = 30 A, Tj = 25°C	–	1.60	2.00	V
VF		FWDi Forward Voltage	VIN = 0 V, IF = 30 A, Tj = 25°C	–	1.70	2.10	
HS	ton	High Side Switching Times	VPN = 600 V, VDD(XX) = 15 V, VBS(X) = 15 V, Ic = 30 A, Tj = 25°C, HIN(X) = 0 V ↔ 5 V, Inductive Load (Note 7) See Figure 9	1.00	1.30	1.90	μs
	tc(on)			–	0.17	0.55	
	toff			–	1.90	2.70	
	tc(off)			–	0.23	0.30	
	trr			–	0.22	–	
LS	ton	Low Side Switching Times	VPN = 600 V, VDD(XX) = 15 V, VBS(X) = 15 V, Ic = 30 A, Tj = 25°C, LIN(X) = 0 V ↔ 5 V, Inductive Load (Note 7) See Figure 9	1.00	1.30	1.90	μs
	tc(on)			–	0.22	0.55	
	toff			–	1.70	2.00	
	tc(off)			–	0.24	0.30	
	trr			–	0.28	–	
Ices		Collector – Emitter Leakage Current	Vce = Vces, Tj = 25°C	–	–	1	mA
BOOTSTRAP CIRCUIT PART							
VF		Forward Voltage	If = 0.1 A, Tj = 25°C	2.1	2.5	2.9	V
RBOOT		Built−in Limiting Resistance		12.5	15.5	18.5	Ω

ELECTRICAL CHARACTERISTICS (VDD = 15 V and Tj = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
CONTROL PART							
IQDDH	Quiescent VDD Supply Current	VDD(xH) = 15 V, HIN(X), LIN(X) = 0 V	VDD(xH) – VSS	–	–	0.30	mA
IQDDL		VDD(L) = 15 V, HIN(X), LIN(X) = 0 V	VDD(L) – VSS	–	–	2.0	
IQBS	Quiescent VBS Supply Current	VB(X) – VS(X) = 15 V, HIN (X) = 0 V	VB(X) – VS(X)	–	–	0.30	
VFOH	Fault Output Voltage	CIN = 0 V, 10 kΩ Pulled up to 5 V		4.9	–	–	V
VFOL		CIN = 1 V, 10 kΩ Pulled up to 5 V		–	–	0.95	
VCIN(ref)	Over Current Trip Level (Note 8)	VDD = 15 V	CIN – VSS	0.46	0.48	0.50	V
UVDDD	Supply Circuit, Under–Voltage Protection	Detection Level		10.3	–	12.5	V
UVDDR		Reset Level		10.8	–	13.0	
UVBSD		Detection Level		10.0	–	12.0	
UVBSR		Reset Level		10.5	–	12.5	
tFOD	Fault–Out Pulse Width	CFOD = 22 nF (Note 9)		1.6	2.4	–	ms
VTS	Voltage Output for LVIC Temperature Sensing Unit (Note 10)	VDD(L) = 15 V, VTS – VSS = 5.1 kΩ, TLVIC = 25°C		1.12	1.25	1.38	V
VIN(ON)	ON Threshold Voltage	Applied between HIN(X), LIN(X) – VSS		–	–	2.6	V
VIN(OFF)	OFF Threshold Voltage			0.8	–	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at Tj = Ta = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible. Values based on design and/or characterization.

7. ton and toff include the propagation delay time of the internal drive IC. tc(on) and tc(off) are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see and Figure 9.
8. Short–circuit current protection is functioning only at the low–sides.
9. The fault–out pulse width tFOD depends on the capacitance value of CFOD according to the following approximate equation: The fault–out pulse width – tFOD = 0.11 x 10^6 x CFOD [s].
10. TLVIC is the temperature of LVIC itself. VTS is only for sensing temperature of LVIC and cannot shutdown IGBTs automatically.

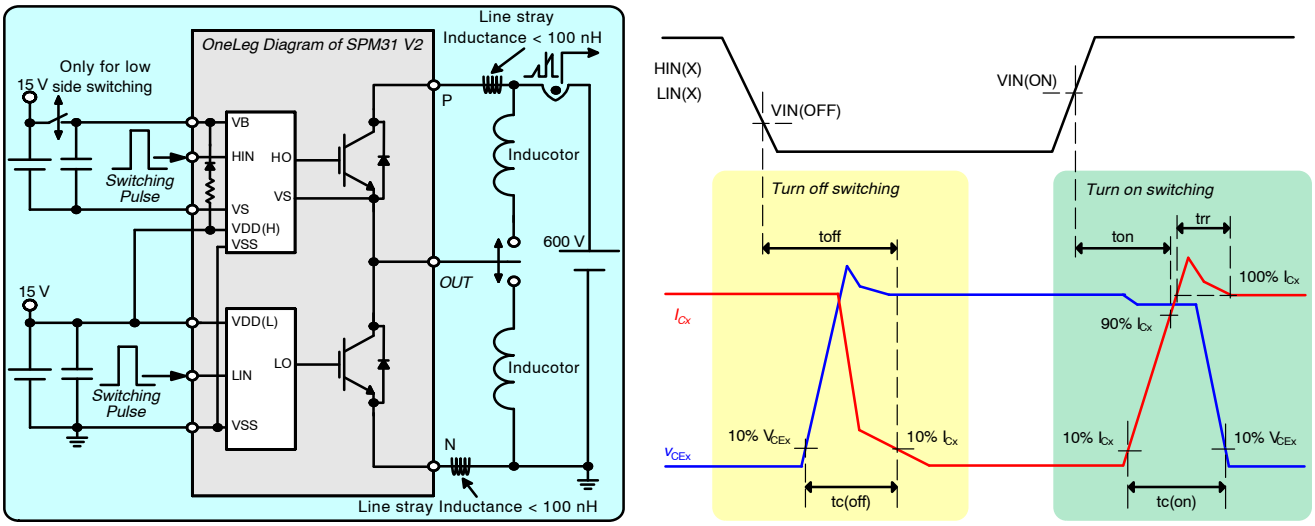


Figure 9. Switching Evaluation Circuit and Switching Time Definition

RECOMMENDED OPERATING CONDITIONS (BASE ON NFAM3512L7B)

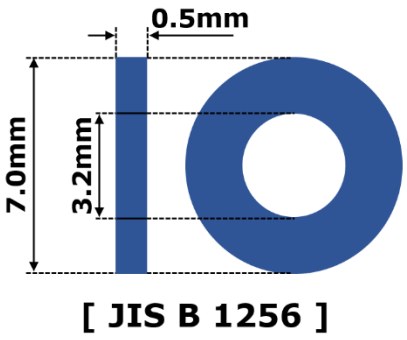
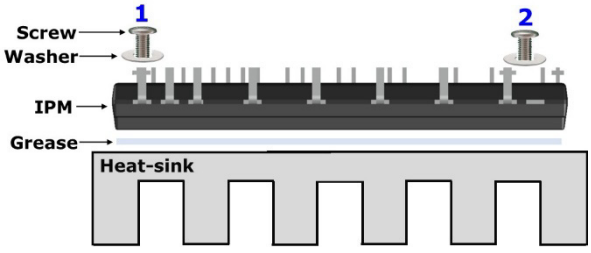
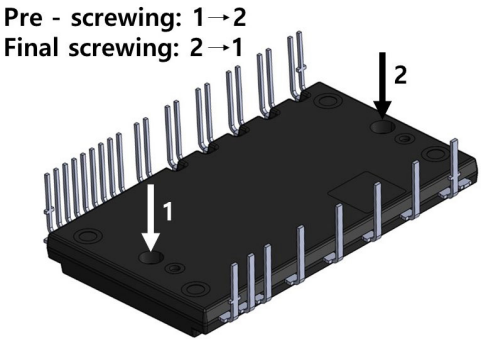
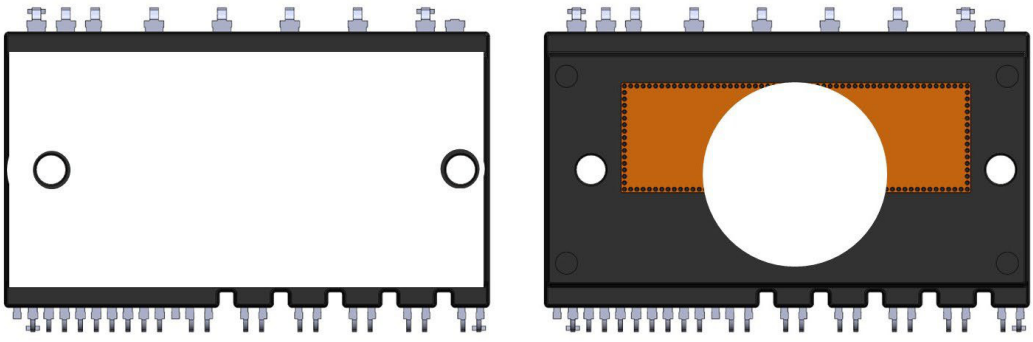
Symbol	Parameter	Condition		Min	Typ	Max	Unit
VPN	Supply Voltage	Applied between P – N_x		–	600	800	V
VDD	Control Supply Voltages	Applied between VDD(XH) – VSS		13.5	15.0	16.5	
VBS	High-Side Bias Voltage	Applied between VB(X) – VS(X)		13.0	15.0	18.5	
dVDD / dt, dVBS / dt	Supply Voltage Variation			–1	–	1	V/μs
Tdead	Blanking Time for Preventing Arm–Short	For Each Input Signal		2.0	–	–	μs
fPWM	PWM Frequency	–40°C ≤ Tc ≤ 125°C, –40°C ≤ Tj ≤ 150°C		2.0	–	20	kHz
Io	Allowable r.m.s Current (Note 11)	VPN = 600 V, VDD = VBS = 15 V, P.F = 0.8, Tc ≤ 125°C, Tj ≤ 150°C	fPWM = 5 kHz	–	–	27.5	Arms
			fPWM = 15 kHz	–	–	18.2	
PWIN(ON)	Minimum Input Pulse Width (Note 12)	VDD = VBS = 15 V, Wiring Inductance between NU, NV, NW and DC Link N < 10 nH		1.0	–	–	μs
PWIN(OFF)				2.0	–	–	
Package Mounting Torque		M3 Type Screw		0.6	0.7	0.9	Nm

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Flatness tolerance of the heatsink should be within –50 μm to +100 μm.

11. Allowable output current value is the reference data for the safe operation of this product. This may be different from the actual application and operating conditions.
12. Product might not make response if input pulse width is less than the recommended value.

MECHANICAL CHARACTERISTICS

Item	Recommended Condition
Pitch	46.0 ±0.1 mm (Please refer to Package Outline Diagram)
Screw	Diameter: M3 Screw head types: pan head, truss head, binding head
Washer	Plane washer dimensions  [JIS B 1256]
Heat sink	Material: Aluminum or Copper Warpage (the surface that contacts IPM): −50 to 100 μm No contamination on the heat sink surface that contacts IPM
Torque	Pre. tightening: 0.2~0.3 Nm on first screw Pre. tightening: 0.2~0.3 Nm on second screw Final tightening: 0.6~0.9 Nm on first screw Final tightening: 0.6~0.9 Nm on second screw  
Grease	Silicone grease. Thickness: 100 to 200 μm Uniformly apply silicon grease on whole IPM TOP surface. Thermal foils are only recommended after careful evaluation. Thickness, stiffness and compressibility parameters have a strong influence on performance.  Recommended Do not recommended

OPERATION SEQUENCE FOR PROTECTIONS

Short Circuit Protection

The 1200 V SPM 31 version 2 series use external shunt resistor for the short circuit current detection, as shown in Figure 10. The LVIC has a built−in short−circuit current protection function that senses the voltage to the CIN pin. If this voltage (VCIN) exceeds the VCIN(ref) (the threshold voltage trip level of over current protection) specified in the device datasheets (VCIN(ref), typ. is 0.48 V), a fault signal is asserted and all three lower side IGBTs are turned off. Short circuit is included to over current situation.

Typically, the maximum short−circuit current magnitude is gate−voltage dependent: higher gate voltage (VDD and VBS) is resulted in a larger short−circuit current. To avoid potential problems, the maximum short−circuit trip level is set below 1.5 times the nominal rated collector current. The LVIC over current protection−timing chart is shown in Figure 11.

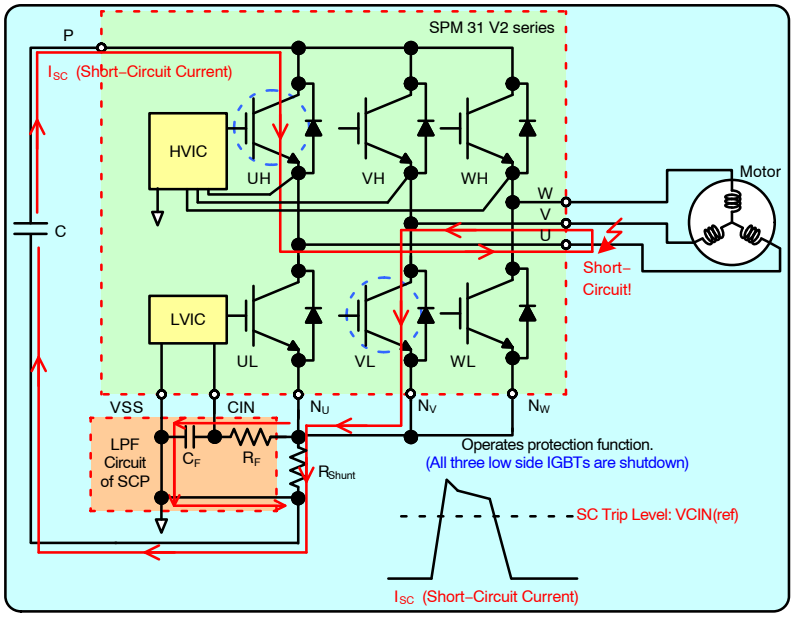
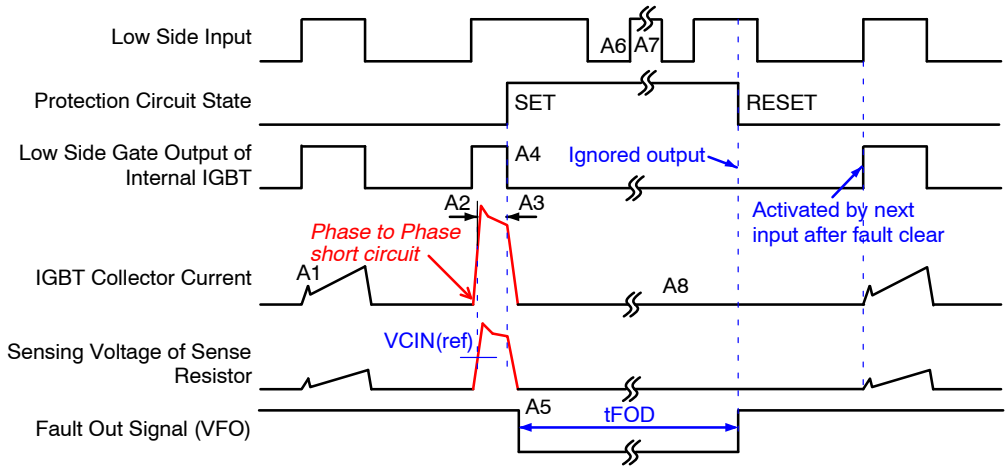


Figure 10. Operation of Short−Circuit Protection



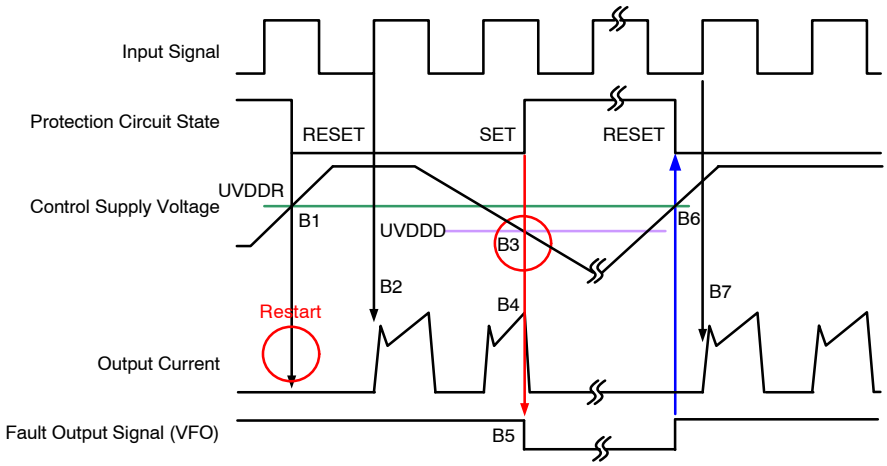
NOTE:

13. A1 − Normal operation: IGBTs turn on and carrying current.
14. A2 − Short circuit current detection (SC trigger).
15. A3 − All low−side IGBT's gate are hard interrupted.
16. A4 − All low side IGBTs turn off.
17. A5 − Fault output timer operation start with internal delay, (Typ. 2.4 ms, CFOD = 22 nF), Fault−out duration time is controlled by CIN.
18. A6 − Input "L": Low side IGBTs OFF state.
19. A7 − Input "H": Low side IGBTs input ON state, but during the active period of fault output the IGBT doesn't turn ON.
20. A8 − Low side IGBTs keeps OFF state.

Figure 11. Timing Chart of Short−Circuit Protection Function

Under−Voltage Lock Out Protection

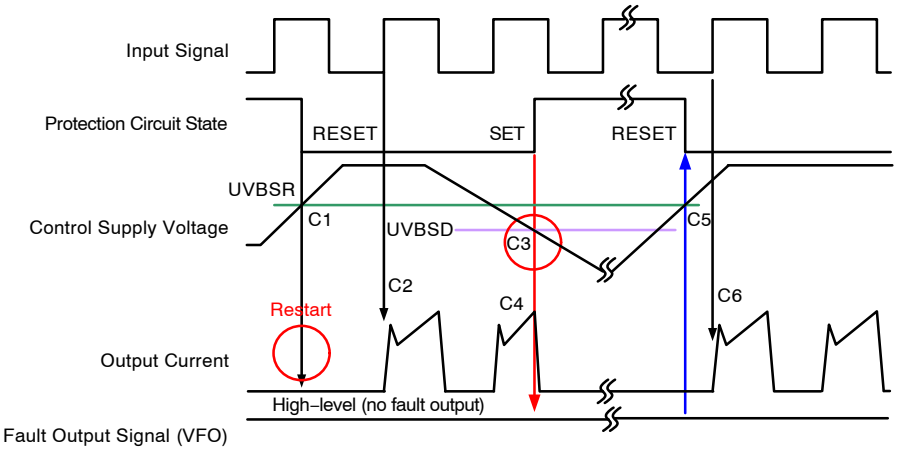
The LVIC has an Under−Voltage Lock Out protection (UVLO) function to protect the low−side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 12.



NOTE:
21. B1 − Control supply voltage rise: after the voltage rises UVDDR, the circuits start to operate when the next input is applied.
22. B2 − Normal operation: IGBT ON and carrying current.
23. B3 − Under−voltage detection (UVDDD).
24. B4 − IGBT OFF in spite of control input is alive.
25. B5 − Fault output signal starts.
26. B6 − Under−voltage reset (UVDDR).
27. B7 − Normal operation: IGBT ON and carrying current. If fault−out duration (tFOD) by external capacitor at CIN pin is longer than UVDDD timing, fault output and IGBT state are cleared after tFOD.

Figure 12. Timing Chart of Low−side Under−Voltage Protection Function

The HVIC has an under-voltage lockout function to protect the high-side IGBT from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 13. A fault−out (VFO) alarm is not given for low at HVIC bias conditions.



NOTE:
28. C1 − Control supply voltage rises: after the voltage reaches UVBSR, the circuit starts when the next input is applied.
29. C2 − Normal operation: IGBT ON and carrying current.
30. C3 − Under−voltage detection (UVBSD).
31. C4 − IGBT OFF in spite of control input is alive, but there is no fault output signal.
32. C5 − Under−voltage reset (UVBSR).
33. C6 − Normal operation: IGBT ON and carrying current.

Figure 13. Timing Chart of High−side Under−Voltage Protection Function

KEY PARAMETER DESIGN GUIDANCE

For stable operation, there are recommended parameters for passive components and bias conditions, considering operating characteristics of the 1200 V SPM 31 version 2 series. This section focuses on the key parameter design guidance.

Circuit of VTS

The Thermal Sensing Unit(VTS) analog voltage output reflects the temperature of the LVIC in 1200 V SPM 31 version 2 series products. The relationship between VTS output voltage and LVIC temperature is shown in Figure 15. It does not have any self−protection function, and, therefore, it should be used appropriately based on application requirement. It should be noted that there is a time lag from IGBT temperature to LVIC temperature. It is very difficult to respond quickly when temperature rises sharply in a transient condition such as shoot−through event. Even though VTS has some limitation, it will be definitely useful in enhancing the system reliability.

Figure 14 shows the LVIC location for VTS function of SPM 31 version 2 series and Figure 15 shows that the relationship between VTS voltage and LVIC temperature.

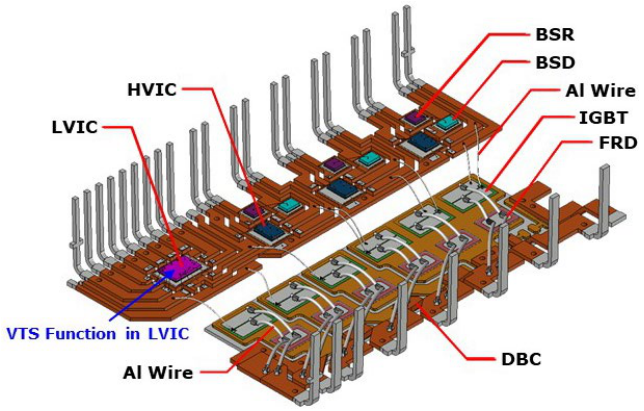


Figure 14. Location of VTS Function (LVIC)

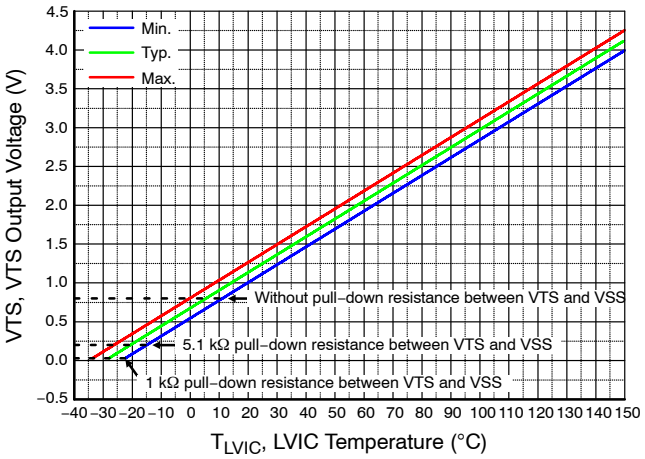


Figure 15. Temperature vs. VTS

Figure 16 shows the equivalent circuit diagram of VTS inside LVIC and a typical application diagram. This output voltage is clamped to 5.2 V by an internal Zener diode, but in case the maximum input range of Analog to Digital converter of MCU is below 5.2 V. An amplifier can be used to change the range of voltage input to MCU to have better resolution of the temperature. It is recommended to add 5.1 kΩ pull−down resistance between VTS and VSS (Signal Ground) as described Figure 16 for linear output characteristics at low temperature. In case of removing pull down resistance between VTS and VSS, VTS output voltage is saturated at 0.8 V and it is normally used under operation conditions over room temperature. To make VTS more stable, a ceramic capacitance of 10 nF is recommended between VTS and VSS as well.

Relationship of VTS and TLVIC can be expressed as the following equation.

$$VTS_{,\,Min} = 0.023 \times T_{LVIC} + 0.545\ (V) \quad \text{(eq. 1)}$$

$$VTS_{,\,Typ} = 0.023 \times T_{LVIC} + 0.675\ (V) \quad \text{(eq. 2)}$$

$$VTS_{,\,Max} = 0.023 \times T_{LVIC} + 0.805\ (V) \quad \text{(eq. 3)}$$

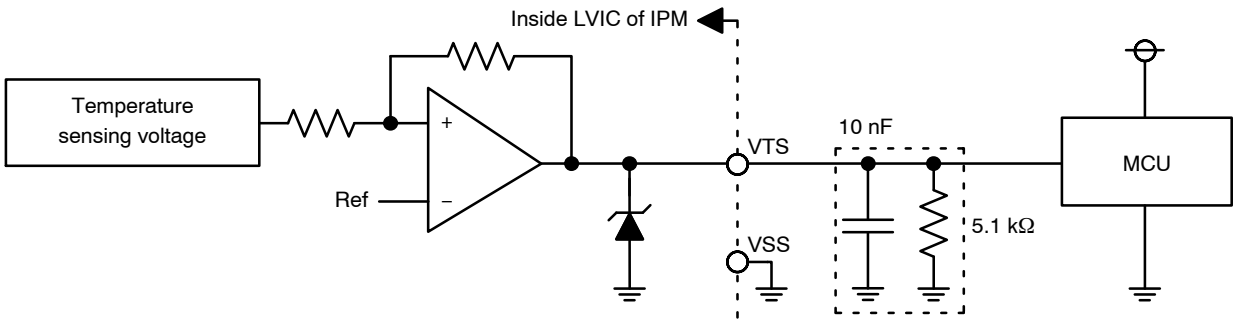


Figure 16. Internal Block Diagram and Interface Circuit of VTS

Selection of Shunt Resistor

Figure 17 shows an example circuit of the short circuit protection using 1-shunt resistor. The line current on the N side DC−ink is detected and the protective operation signal is passed through the RC filter. If the current exceeds the short circuit reference level, all the gates of the N−side three−phase IGBTs are switched to the off state and the VFO fault signal is transmitted to MCU. Since short circuit protection is non−repetitive, IGBT operation should be immediately halted when the VFO fault signal is given.

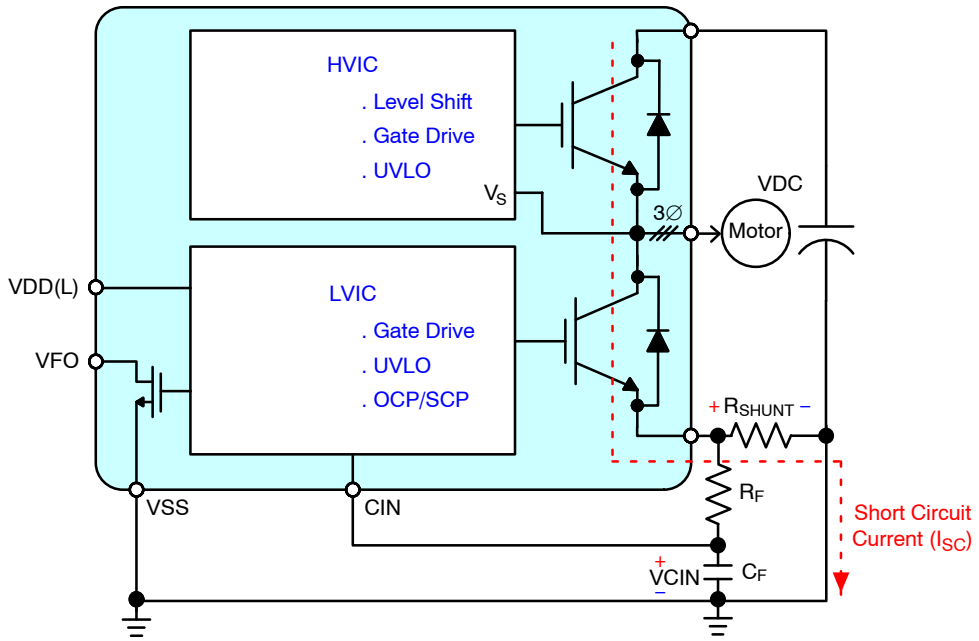


Figure 17. Short Circuit Current Protection Circuit with One Shunt Resistor

The value of shunt resistance is calculated by the following equation.

- Maximum Current Trip Level:
  - ♦ Depends on user selection:
  - − $I_{SC(max)}$ = 1.5 x I_C (Rated current)
- SC trip reference voltage:
  - ♦ Depends on datasheet
  - − VCIN(ref) = Min. 0.46 V, Typ. 0.48 V, Max. 0.50 V
- Shunt resistance:
  - − $I_{SC(max)} = VCIN(Ref.)_{\_Max.} / R_{SHUNT(Min.)} \rightarrow R_{SHUNT(Min.)} = V_{SC(Max.)} / I_{SC(Max.)}$
- If the deviation of the shunt resistor should be limited below ±5%,
  - − $R_{SHUNT(typ)} = VCIN(Ref.)_{\_Typ.} / I_{SC(max)}$,
  - − $R_{SHUNT(Min.)} = R_{SHUNT(Typ.)} \times 0.95$,
  - − $R_{SHUNT(Max.)} = R_{SHUNT(Typ.)} \times 1.05$
- Actual short circuit trip current level becomes:
  - − $I_{SC(Typ.)} = VCIN(Ref)_{\_Typ.} / R_{SHUNT(Typ.)}$
  - − $I_{SC(Min.)} = V_{SC(Min.)} / R_{SHUNT(Max.)}$
- Inverter output power:
  - − $P_{OUT} = \sqrt{3} \times VO,LL \times I_{O(RMS)} \times PF$

Where:

- − $VO,LL = \frac{\sqrt{3}}{\sqrt{2}} \times MI \times \frac{V_{DC}}{2}$
- − $I_{O(RMS)}$ = Maximum load current of inverter
- − M.I = Modulation Index
- − VDC = DC link voltage
- − PF = Power Factor

- Average DC Current
  - $I_{DC\_AVG} = (P_{out} \text{ x Eff}) / V_{DC\_Link}$

  Where:
  - Eff = Inverter Efficiency
- The power rating of shunt resistor is calculated by the following equation
  - $P_{SHUNT} = (I_{RMS}^2 \times R_{SHUNT} \times \text{Margin}) / \text{De−rating Ratio}$

  Where:
  - R_{SHUNT} is shunt resistance typical value at Tc = 25°C
  - De−rating ratio is ratio of shunt resistor at T_{SHUNT} = 100°C (From datasheet of shunt resistor)
  - Margin is safety margin (Determine by user)
- Shunt resistor calculation examples:
  - ♦ Calculation conditions:
  - DUT: NFAM3512L7B
  - Tolerance of shunt resistor: ±5 %
  - SC Trip Reference Voltage, VCIN(ref):
  - $VCIN(ref)_{\_Min.}$ = 0.46 V, $VCIN(ref)_{\_Typ.}$ = 0.48 V, $VCIN(ref)_{\_Max.}$ = 0.50 V
  - Maximum Load Current of Inverter (I_{RMS}): 25 A_{rms}
  - Maximum Peak Load Current of Inverter (IC(max)): 52.5 A
  - Modulation Index(MI): 0.9
  - DC Link Voltage(VDC_Link): 600 V
  - Power Factor (PF): 0.8
  - Inverter Efficiency(Eff): 0.95
  - Shunt Resistor Value at Tc = 25°C (R_{SHUNT}): 9.1 mΩ
  - De−rating Ration of Shunt Resistor at T_{SHUNT} = 100°C: 70 % (refer to Figure 18)
  - Safety Margin: 20 %
  - ♦ Calculation results:
  - $I_{SC(Max.)}$: 1.5 × $I_{C(Max.)}$ = 1.5 x 35 A = 52.5 A
  - $R_{SHUNT(Typ.)}$: $VCIN(ref)_{\_Typ.}$ / $I_{SC(Max.)}$ = 0.48 V / 52.5 A = 9.1 mΩ
  - $R_{SHUNT(Max.)}$: $R_{SHUNT(Typ.)}$ x 1.05 = 9.1 mΩ x 1.05 = 9.6 mΩ
  - $R_{SHUNT(Min.)}$: $R_{SHUNT(Typ.)}$ x 0.95 = 9.1 mΩ x 0.95 = 8.7 mΩ
  - $I_{SC(Min.)}$: $VCIN(ref)_{\_Min.}$ / $R_{SHUNT(Max.)}$ = 0.46 V / 9.6 mΩ = 47.9 A
  - $I_{SC(Max.)}$: $VCIN(ref)_{\_Max.}$ / $R_{SHUNT(Min.)}$ = 0.5 V / 8.7 mΩ = 57.5 A
  - $P_{OUT} = \sqrt{3} \times \left(\frac{\sqrt{3}}{\sqrt{2}} \text{ x MI x } \frac{V_{DC}}{2} \right) \text{ x } I_{O(RMS)} \times PF = \frac{3}{\sqrt{2}} \times 0.9 \times (600 / 2) \times 25 \times 0.8 = 11{,}455 \text{ W}$
  - $I_{DC\_AVG} = (P_{OUT} \text{ x Eff}) / V_{DC\_Link}$ = 18.14 A
  - $P_{SHUNT} = (I_{DC}^2{}_{\_AVG} \text{ x } R_{SHUNT} \text{ x Margin}) / \text{De−rating Ratio} = ((18.14)^2 \times 0.0091 \times 1.2) / 0.7 = 5.1$ W (therefore, the proper power rating of shunt resistor is over 5.1 W).

When over−current events are detected, the 1200 V SPM 31 version 2 series shuts down all low−side IGBTs and sends out the fault−out (VFO) signal. FAULT output timer operation starts with internal delay (typ. 2.4 ms, CFOD = 22 nF), Fault−out duration time is controlled by CFOD.

To prevent malfunction, it is recommended that an RC filter is inserted between Nx and CIN pin. To shut down IGBTs within 3 μs when over−current situation occurs, a time constant of 1.5~2 μs is recommended.

Table 3 shows the shunt resistance by typical current level of short−circuit protection for each product.

Table 3. OVER−CURRENT (OC) PROTECTION TRIP LEVEL

Device	R_{SHUNT}	Over Current Trip Level	Remark
NFAM1512L7B	21.3 mΩ	22.5 A	Typical value
NFAM2512L7B	12.8 mΩ	37.5 A	
NFAM3512L7B	9.1 mΩ	52.5 A	
NFAM4012L7B	8.0 mΩ	60.0 A	

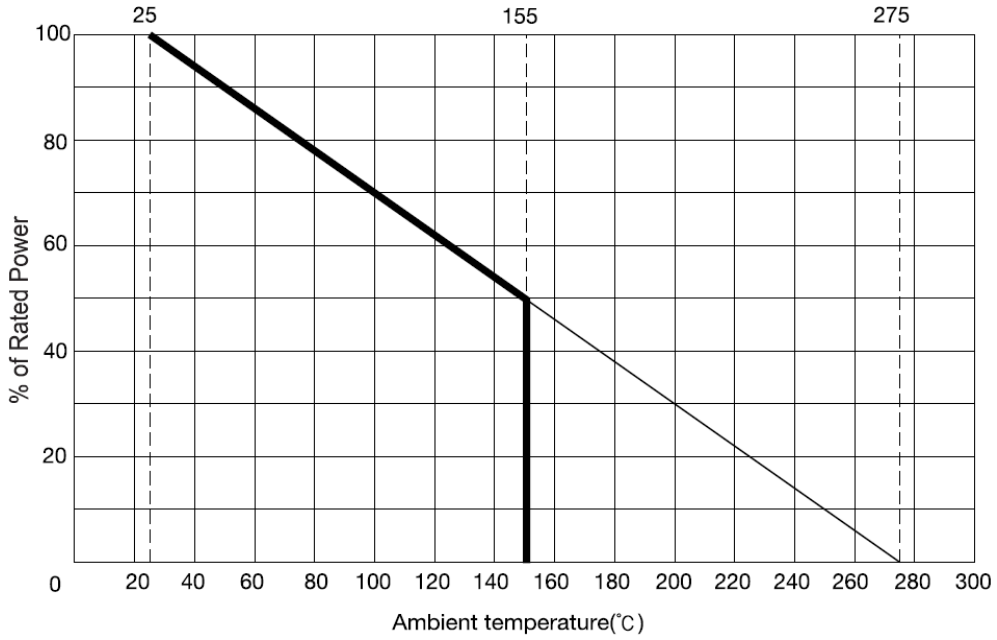


Figure 18. De−rating Curve Example of Shunt Resistor (from RARA Elec.)

Time Constant of Internal Delay

An RC filter prevents unexpected malfunction by related noise such as current protection and short circuit current protection (OCP, SCP) situation. The RC time constant is determined by the applied noise time and the Short−Circuit Withstanding Time (SCWT) of SPM 31 version 2 series. When the voltage of R_{shunt} exceeds the VCIN(ref) level, It is applied to the CIN pin via the RC filter. The RC filter delay is the time required for the CIN voltage to rise to the referenced over current protection level. The LVIC has an internal filter time (logic filter time for noise elimination: around 0.85 μs). User should consider this filter time when they design the RC filter between shunt resistor and CIN pin. Figure 19 shows timing diagram of over current protection and short circuit protection. Measured time is shown Table 4. User should be considering each time sections for distribution under protection situation.

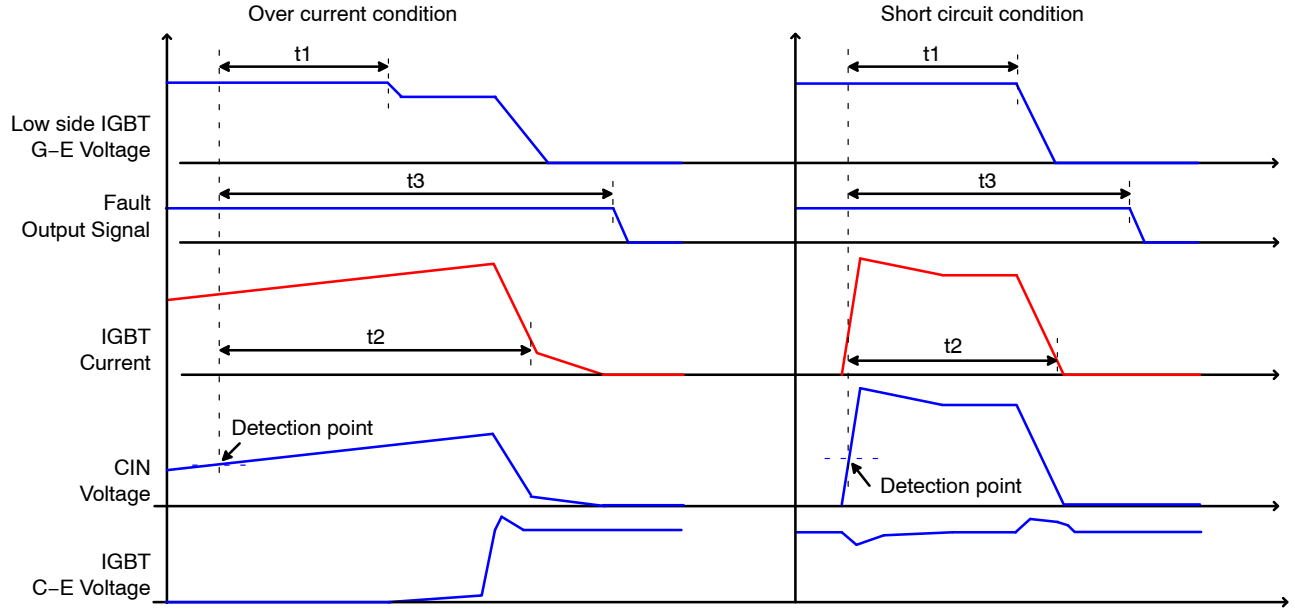


Figure 19. Timing Diagram of Over and Short Circuit Protection

Table 4. TIME TABLE OF O.C AND S.C PROTECTION; VCIN(ref) TO LOW SIDE GATE, COLLECTOR CURRENT AND VFO

Ref. Condition VPN = 600 V, VDD = 15 V		Over Current (2 x Rated Current)						Short Circuit					
		t1 (μs) (Note 34)		t2 (μs) (Note 35)		t3 (μs) (Note 36)		t1 (μs) (Note 34)		t2 (μs) (Note 35)		t3 (μs) (Note 36)	
Device	**Tj (°C)**	**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**
NFAM1512L7B	**25**	1.05	1.30	1.25	1.55	4.00	5.00	1.05	1.30	1.15	1.45	4.00	5.00
	150	1.00	1.25	1.30	1.60	3.20	4.20	1.00	1.25	1.20	1.50	3.20	4.20
NFAM2512L7B	**25**	1.05	1.30	1.30	1.60	4.00	5.00	1.05	1.30	1.20	1.50	4.00	5.00
	150	1.00	1.25	1.35	1.65	3.20	4.20	1.00	1.25	1.25	1.55	3.20	4.20
NFAM3512L7B	**25**	1.05	1.30	1.35	1.65	4.00	5.00	1.05	1.30	1.25	1.55	4.00	5.00
	150	1.00	1.25	1.40	1.75	3.20	4.20	1.00	1.25	1.30	1.65	3.20	4.20

To guarantee safe short−circuit protection under all operating conditions, VCIN should be detected within 1.0 μs after short circuit occurs. (Recommendation: SCWT < 3.0 μs, Conditions: VDC = 800 V, VDD = 16.5 V, Tj = 150°C).
It is recommended that delay time should be minimized from short−circuit to CIN triggering
34. t1: from CIN detection to gate driver LO shut down
35. t2: from CIN detection to collector current 10 %
36. t3: from CIN detection to fault out signal activation

Fault Output Circuit

VFO pin is the fault output alarm pin to give a fault state condition in SPM31 version 2 products. And an active low output is given on this pin for a fault state condition. The alarm conditions are Over−Current Protection (OCP), or low−side bias Under−Voltage Lock Out (UVLO) operation. The VFO output is open drain configured and VFO signal line should be pulled up to control power supply with 10 kΩ resistance as shown in Figure 20. The RC coupling shown dotted in Figure 20 can be changed depending on the application and the wiring impedance.

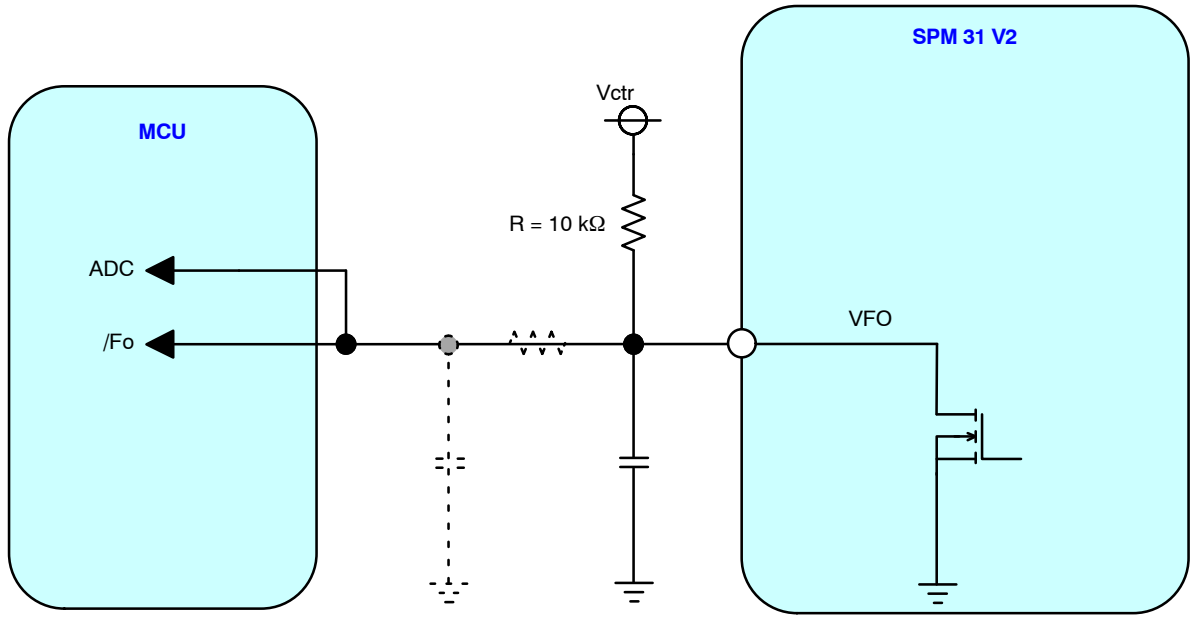


Figure 20. Propose Circuit for Fault Output Function

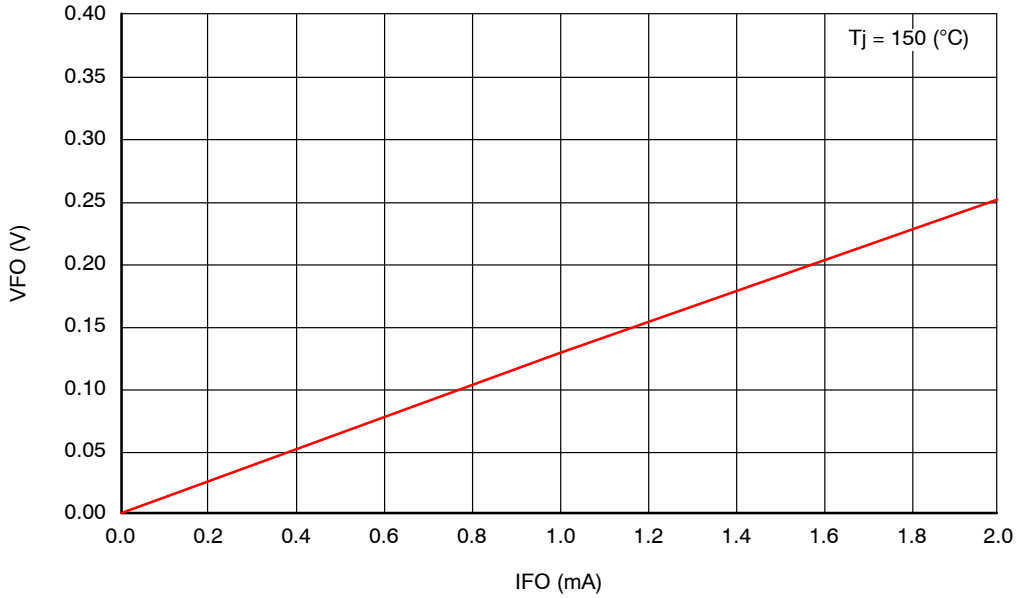


Figure 21. Voltage−Current Characteristics of VFO Terminal

Circuit of Input Signal (HINx, LINx)

Figure 22 shows recommended I/O interface circuit between the MCU and SPM 31 version 2. Because SPM 31 version 2 input logic is active HIGH and there are built−in pull−down resistors, external pull−down resistors are not needed.

Since the fault output is open drain and its rating is VDD + 0.3 V, 15 V supply interface is possible.

However, it is recommended that the fault output is configured with the 5 V logic supplies, which is the same as the input signals. It is also recommended that the decoupling capacitors is placed at both the MCU and Motion SPM 31 version 2 ends of the VFO signal line, as close as possible to each device. The RC coupling at each input (parts shown dotted in Figure 22) can be changed depending on the PWM control scheme used in the application and the wiring impedance of the PCB layout.

The input signal section of the SPM 31 version 2 series integrates a 5 kΩ (typical) pull−down resistor. Therefore, when using an external filtering resistor between the MCU output and the Motion SPM 31 version 2 input, attention should be given to the signal voltage drop at the Motion SPM 31 version 2 input terminals to satisfy the turn−on threshold voltage requirement. For instance, R = 100 Ω and C = 1 nF for the parts shown dotted in Figure 22.

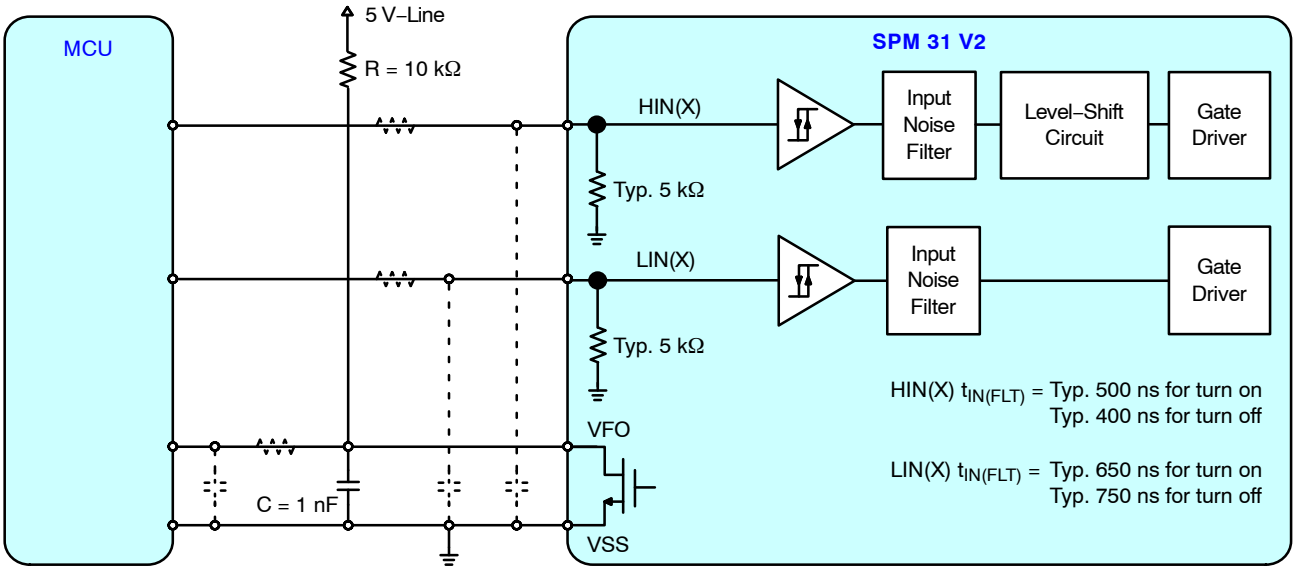


Figure 22. Recommended MCU I/O Interface Circuit

Bootstrap Circuit Design

Operation of Bootstrap Circuit

The VBS voltage, which is the voltage difference between VB(U,V,W) and VS(U,V,W), provides the supply to the HVIC within the 1200 V SPM 31 version 2 series. This supply must be in the range of 13.0 V~18.5 V to ensure that the HVIC can fully drive the high−side IGBT. The SPM 31 version 2 series includes an under−voltage lock out protection function for the VBS to ensure that the HVIC does not drive the high−side IGBT, if the VBS voltage drops below a specified voltage. This function prevents the IGBT from operating in a high dissipation mode. There are a number of ways in which the VBS floating supply can be generated. One of them is the bootstrap method described here (refer to Figure 23). This method has the advantage of being simples and inexpensive. However, the duty cycle and on−time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap to ground (either through the low−side or the load), the bootstrap capacitor (C_{BOOT}) is charged through the bootstrap diode (D_{BOOT}) and the resistor (R_{BOOT}) from the VDD supply.

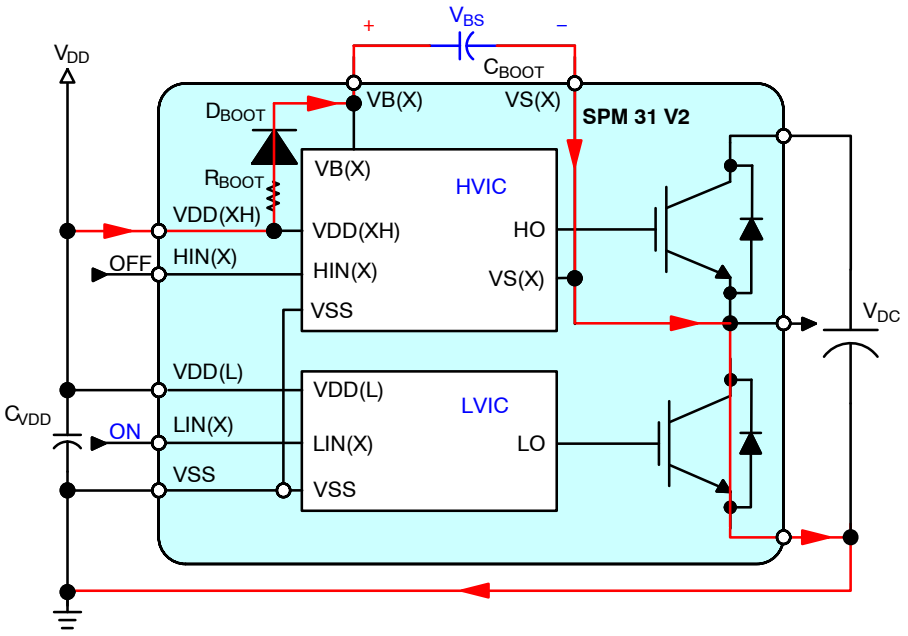


Figure 23. Current Path of Bootstrap Circuit

Selection of Bootstrap Capacitor Considering Initial Charging

Adequate on−time duration of the low−side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated by:

$$t_{charge} = C_{BOOT} \times R_{BOOT} \times \frac{1}{\delta} \times \ln \frac{VDD}{VDD - VBS(Min) - VF - VLS} \quad \text{(eq. 4)}$$

Where:
VF = Forward voltage drop across the bootstrap diode;
VBS(Min.) = The minimum value of the bootstrap capacitor;
VLS = Voltage drop across the low−side IGBT or load; and
“δ” = Duty ratio of PWM.

Charging bootstrap capacitor is initially required before normal operation of PWM starts for the SPM 31 version 2 series. When the bootstrap capacitor is charged initially; VDD drop voltage is generated based on initial charging method, VDD line SMPS output current, VDD source capacitance, and bootstrap capacitance. If VDD drop voltage reaches UVDDD level, the low side is shut down and a fault signal is activated.

To avoid this malfunction, related parameter and initial charging method should be considered. To reduce VDD voltage drop at initial charging, a large VDD source capacitor and selection of optimized low−side turn−on method are recommended.

Figure 24 shows an example of initial bootstrap charging sequence. Once VDD establishes, VBS needs to be charged by turning on the low−side IGBTs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval, based on the switching carrier frequency.

Therefore, it is desired to maintain this structure without creating complementary high−side PWM signals. The capacitance of VDD should be sufficient to supply necessary charge to VBS capacitance in all three phases. If a normal PWM operation starts before VBS reaches UVLO reset level, the high−side IGBTs cannot switch without creating a fault signal. It may lead to a failure of motor start in some applications. If three phases are charged synchronously, initial charging current through a single shunt resistor may exceed the over−current protection level.

Therefore, initial charging time for bootstrap capacitors need to be separated, as shown in Figure 25 if amount of initial current during short time should be minimized. The effect of the bootstrap capacitance factor and charging method (low−side IGBT driving method) is shown in Figure 24.

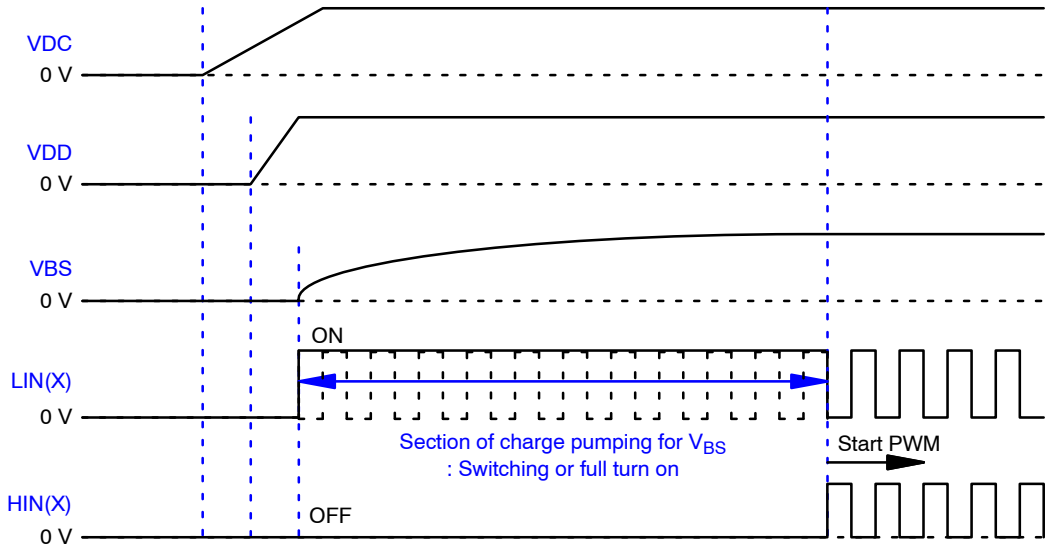


Figure 24. Timing Chart of Initial Bootstrap Charging

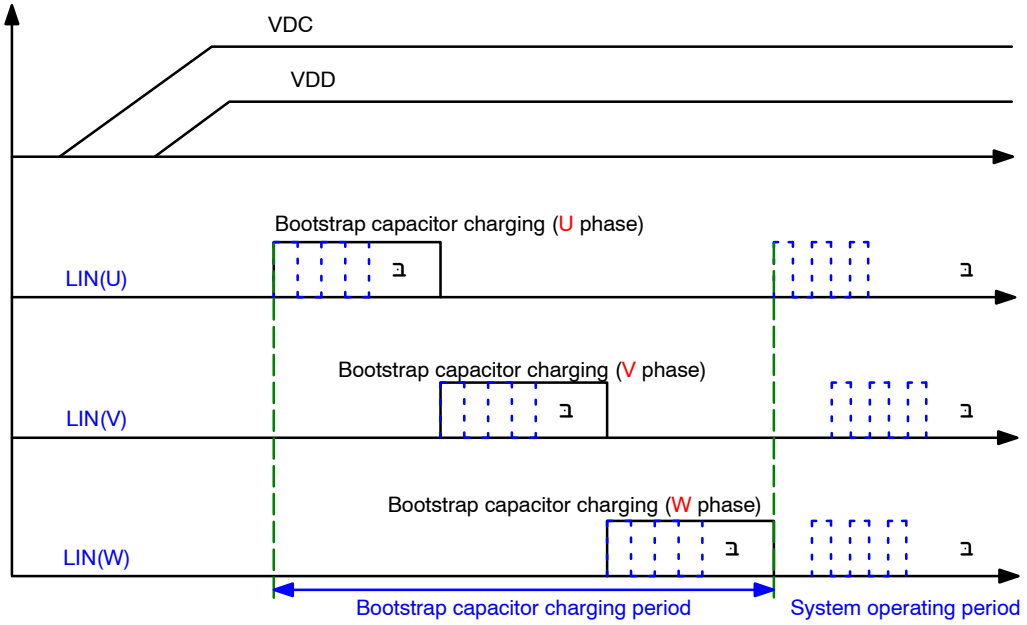


Figure 25. Recommended Initial Bootstrap Capacitors Charging Sequence

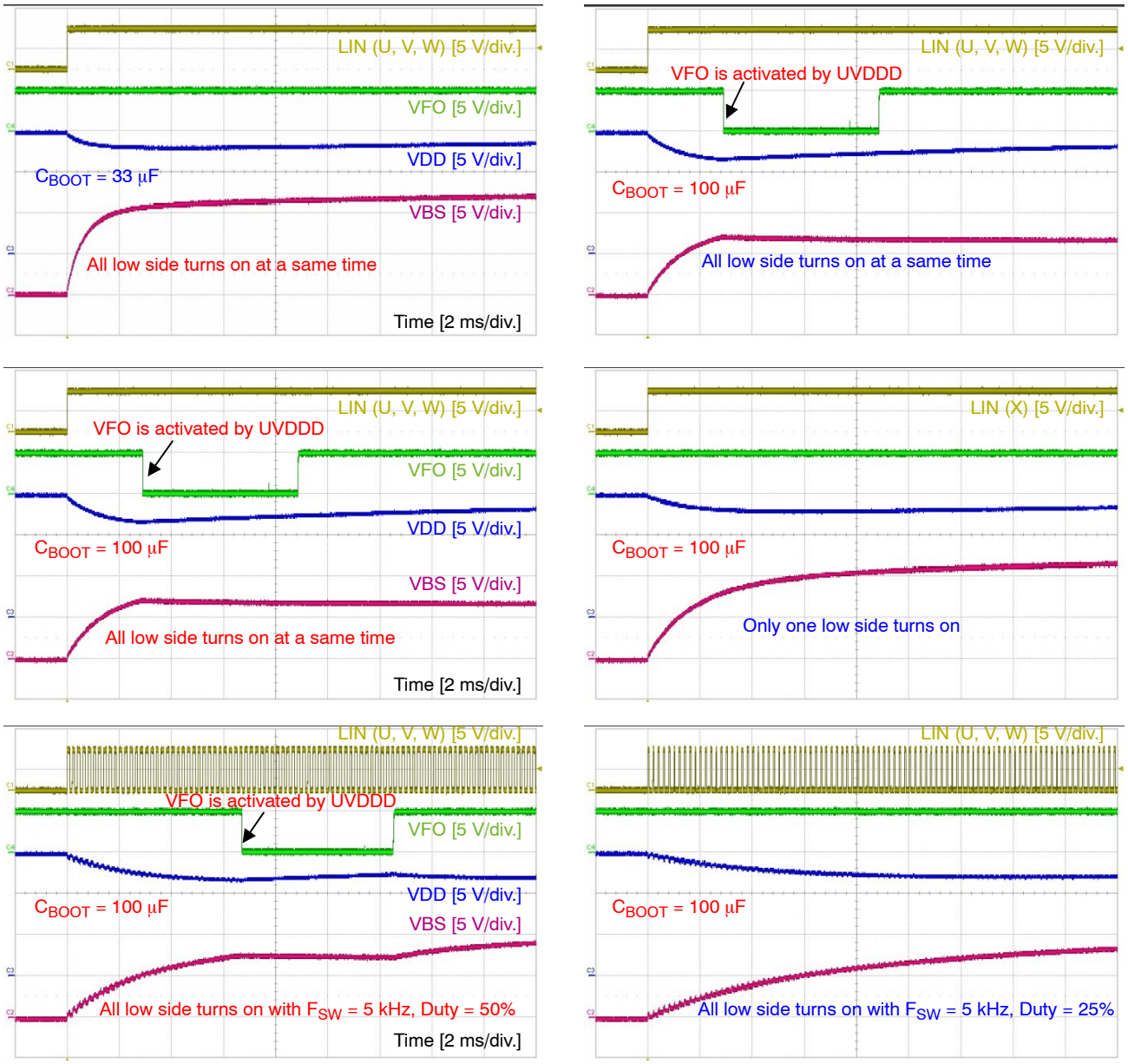


Figure 26. Initial Charging According to Bootstrap Capacitance and Charging Method (Ref. Condition: VDD = 15 V / 300 mA, VDD Capacitor = 220 μF, C_{BOOT} = 100 μF, R_{BOOT} = 20 Ω)

Selection of Bootstrap Capacitor Considering Operating

The bootstrap capacitance can be calculated by:

$$C_{BOOT} = \frac{I_{Leak} \times \Delta t}{\Delta VBS} \quad \text{(eq. 5)}$$

Where:

Δt: Maximum on pulse width of high−side IGBT;

ΔVBS: The allowable discharge voltage of the C_{BOOT} (voltage ripple); and

I_{Leak}: Maximum discharge current of the C_{BOOT}.

Mainly via the following mechanisms:

- Gate charge for turning the high−side IGBT on.
- Quiescent current to the high−side circuit in HVIC.
- Level−shift charge required by level−shifters in HVIC.

- Leakage current in the bootstrap circuit.
- C_{BOOT} capacitor leakage current (ignored for non−electrolytic capacitors).
- Bootstrap diode reverse recovery charge.

Practically, 3.5 mA of I_{Leak} is recommended for the 1200 V SPM 31 version 2 series. By considering dispersion and reliability, the capacitance is generally selected to be 2~3 times of the calculated one. The C_{BOOT} is only charged when the high−side IGBT is off and the VS(x) voltage is pulled down to ground.

The on−time of the low−side IGBT must be sufficient to ensure that the charge drawn from the C_{BOOT} capacitor to be fully replenished. This creates an inherent minimum on−time of the low−side IGBT (or off−time of the high−side IGBT).

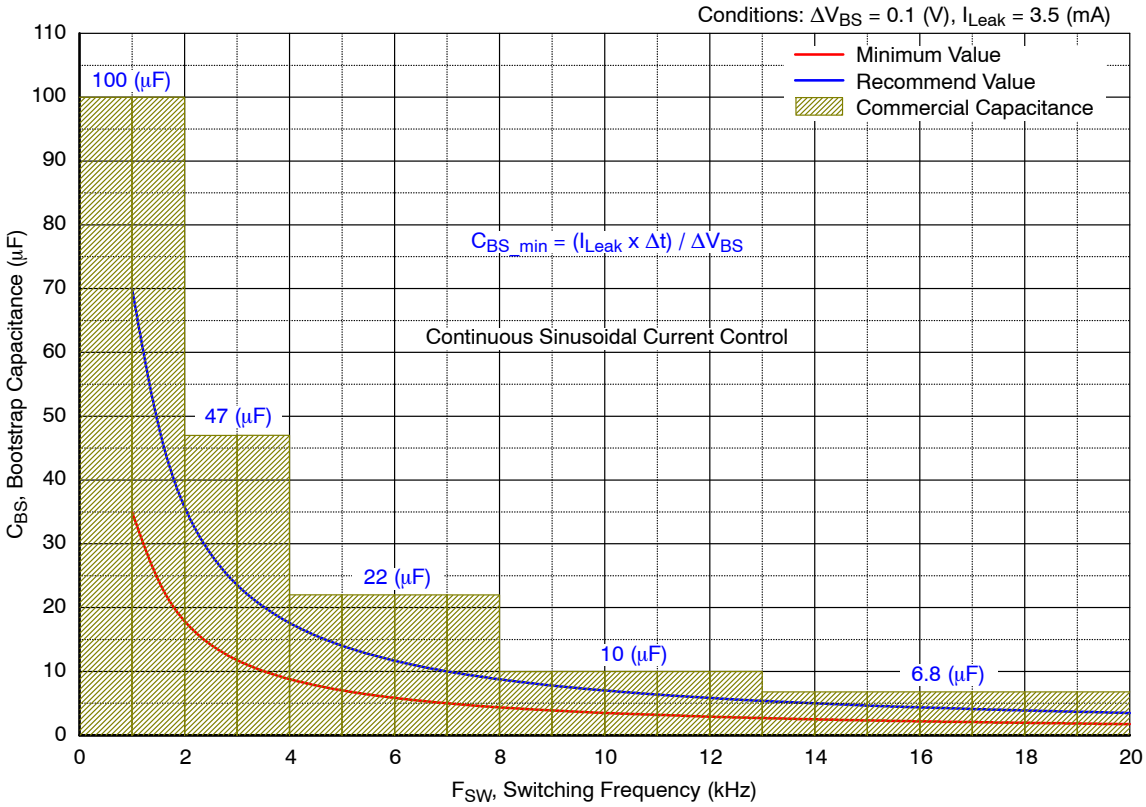


Figure 27. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

Based on switching frequency and recommended ΔVBS.
I_{Leak}: circuit current = 3.5 mA (recommended value)
ΔVBS: discharged voltage = 0.1 V (recommended value)
Δt: maximum on pulse width of high−side IGBT = 0.2 ms (depends on application)

NOTE:
37. The capacitance can be changed according to the switching frequency, capacitor type, and VBS voltage. The above result is a calculation example. So, This value can be changed according to the control method and lifetime of the component.

Built−in Bootstrap Circuit

When the low−side IGBT or diode conducts, the bootstrap diode (D_{BOOT}) supports the entire bus voltage. Hence, a diode with withstand voltage of more than 1200 V is recommended. It is important that this diode has a fast recovery (recovery time < 100 ns) characteristic to minimize the amount of charge fed back from the bootstrap capacitor into the VDD supply. The bootstrap resistor (R_{BOOT}) is to slow down the dVBS/dt and limit initial charging current (I_{charge}) of bootstrap capacitor.

Normally, a bootstrap circuit consists of bootstrap diode (D_{BOOT}), bootstrap resistor (R_{BOOT}), and bootstrap capacitor (C_{BOOT}). As shown in Figure 28, the built−in bootstrap circuit of SPM 31 version 2 product has special VF characteristics with bootstrap resistor. Therefore, only external bootstrap capacitors are needed to make bootstrap circuit.

The characteristics of the built−in bootstrap diode in the SPM 31 version 2 products are:

Fast recovery diode: more than 1200 V / 2 A

Resistive characteristic: equivalent resistor of approximately 15.5 Ω

Table 5 shows the specification of bootstrap circuit. Figure 28 shows forward voltage drop of the bootstrap diode.

Table 5. SPECIFICATION FOR INTEGRATED BOOTSTRAP CIRCUIT

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VF	Forward Voltage	If = 0.1 A, Tj = 25°C	2.1	2.5	2.9	V
RBOOT	Built−in Limiting Resistance		12.5	15.5	18.5	Ω

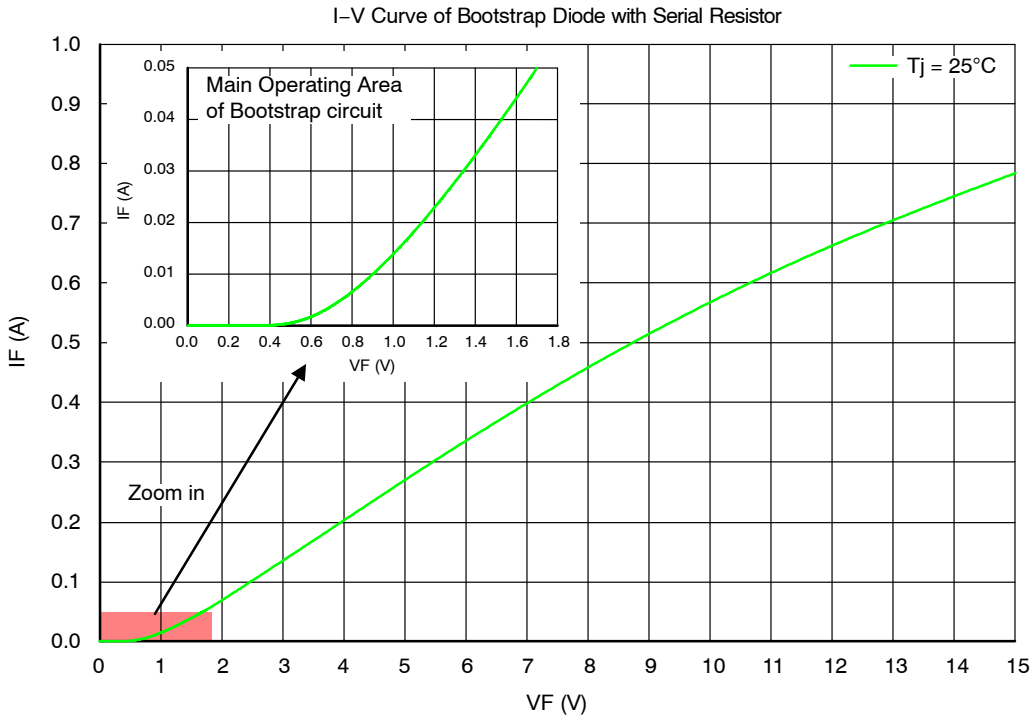
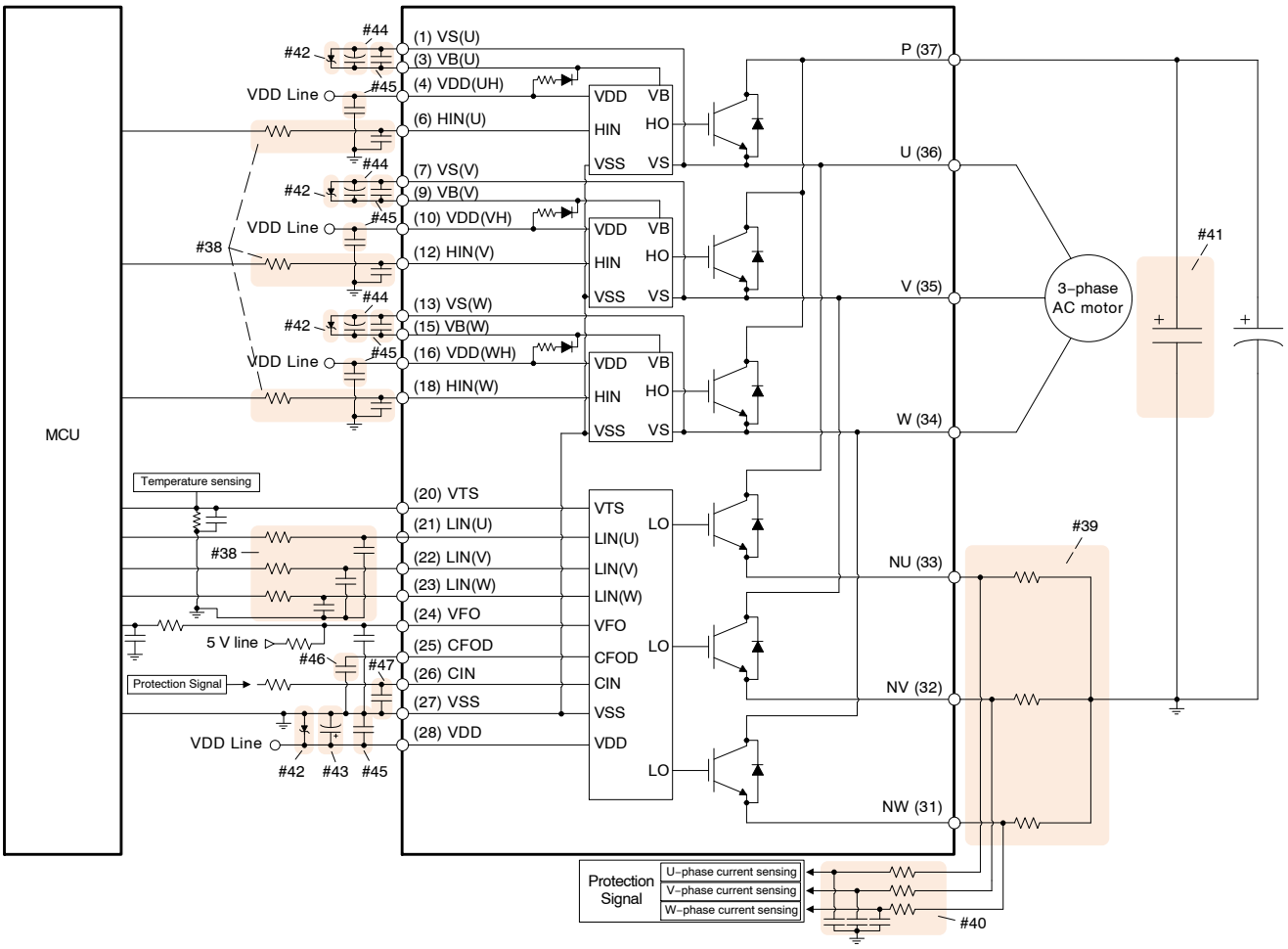


Figure 28. V−I Characteristics of Bootstrap Circuit in SPM 31 Version 2 Series Products

PRINT CIRCUIT BOARD (PCB) DESIGN

General Application Circuit Example

Figure 29 shows a general application circuitry of interface schematic with control signals connected directly to MCU. Figure 30 shows guidance of PCB layout for the 1200 V SPM 31 version 2 series.



To avoid malfunction, the wiring of each input should be as short as possible (less than 2−3 cm). Each capacitor should be mounted as close to the pins of the product as possible. VFO output is open−drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes IFO up to 1 mA. Please refer to Figure 22.

NOTE:

38. Input signal is active−HIGH type. There is a 5 kΩ resistor inside the IC to pull−down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. RC time constant should be selected in the range 50~150 ns. (Recommended R = 100 Ω, C = 1nF)
39. Each wiring pattern inductance should be minimized (Recommend less than 10 nH). Use the shunt resistor of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring should be connected to the terminal of the shunt resistor as close as possible.
40. In the short−circuit protection circuit, please select the RC time constant in the range 1.5~2.0 μs. Do enough evaluation on the real system because short−circuit protection time may vary wiring pattern layout and value of the RC time constant.
41. To prevent surge destruction, the wiring between the snubber capacitor and the P & GND pins should be as short as possible. The use of a high−frequency non−inductive capacitor of around 0.1~0.22 μF between the P & GND pins is recommended.
42. The zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (Recommended zener diode is 22 V / 1 W, which has the lower zener impedance characteristic than about 15 Ω).
43. VDD electrolytic capacitor is recommended around 7 times larger than VBS electrolytic bootstrap capacitor.
44. Please choose the VBS electrolytic bootstrap capacitor with good temperature characteristic.
45. 0.1~0.2 μF R−category ceramic capacitors with good temperature and frequency characteristics is recommended.
46. Fault out pulse width can be adjusted by capacitor connected to the CFOD terminal.
47. To prevent protection function errors, CIN capacitor should be placed as close to CIN and VSS pins as possible.

Figure 29. General Application Circuitry for 1200 V Motion SPM 31 Version 2

PCB Layout Guidance

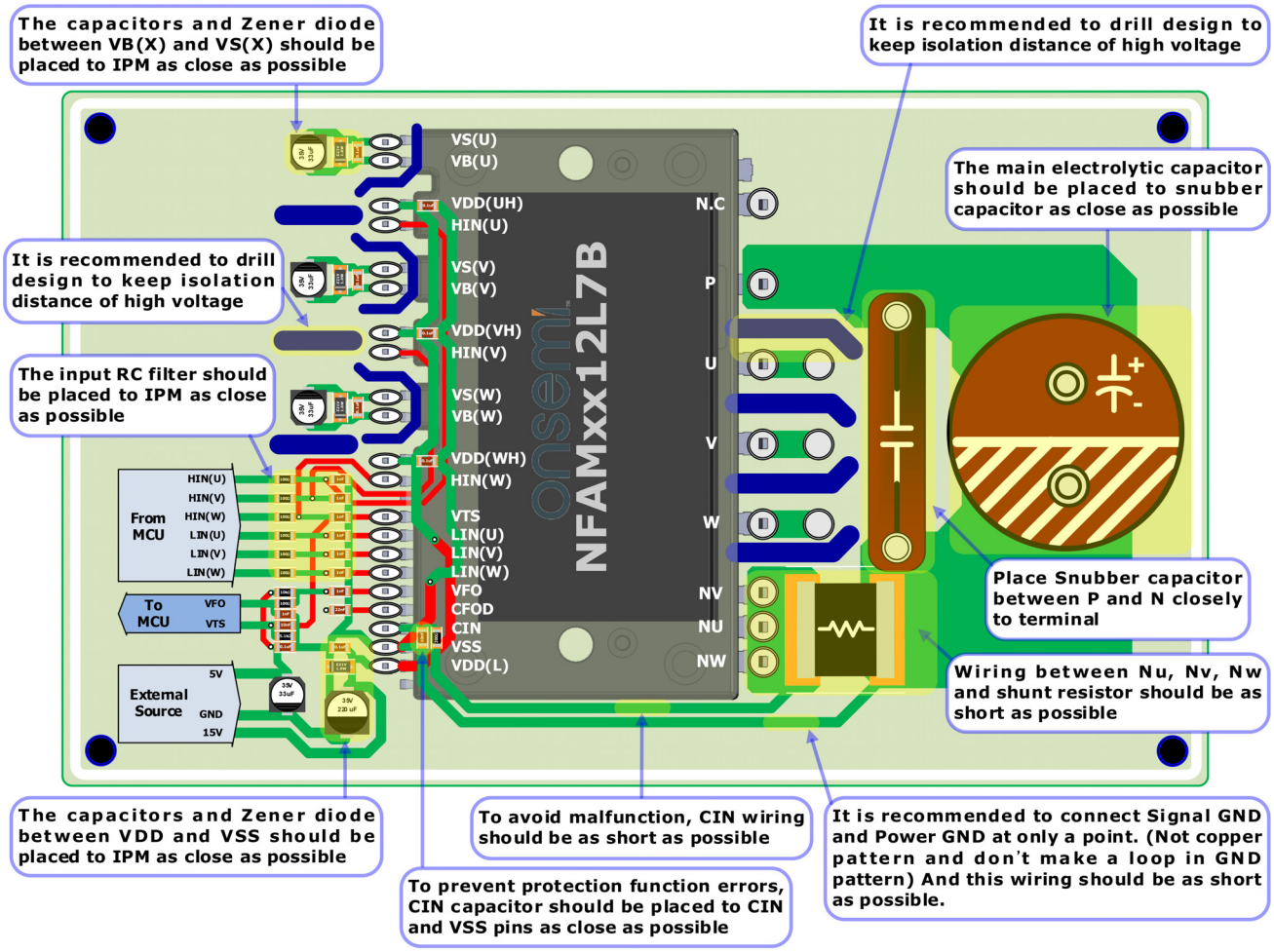


Figure 30. Print Circuit Board (PCB) Layout Guidance for SPM 31 Version 2 Series

REVISION HISTORY

Revision	Description of Changes	Date
O	Initial document version release.	12/06/2023
OX	p27 (#42, #44 components direction in Figure 29)	12/07/2023
OXX	p15 (Fig. 13 name corrected), p16 (Eq. 2, 3 corrected)	11/14/2023
OXXX	change / to “x” Formula on page 17	6/27/2025

ADDITIONAL INFORMATION

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